

# Winery CALPELLA N11M-GE Schematics

Mobile Arrandale

Intel Ixex Peak-M

2009-09-09

REV : SA

*DY : Nopop Component*

*UMA : Pop when schematic is UMA*

*DIS : Pop when schematic is DIS*

# Winery CALPELLA Block Diagram

## PCB LAYER

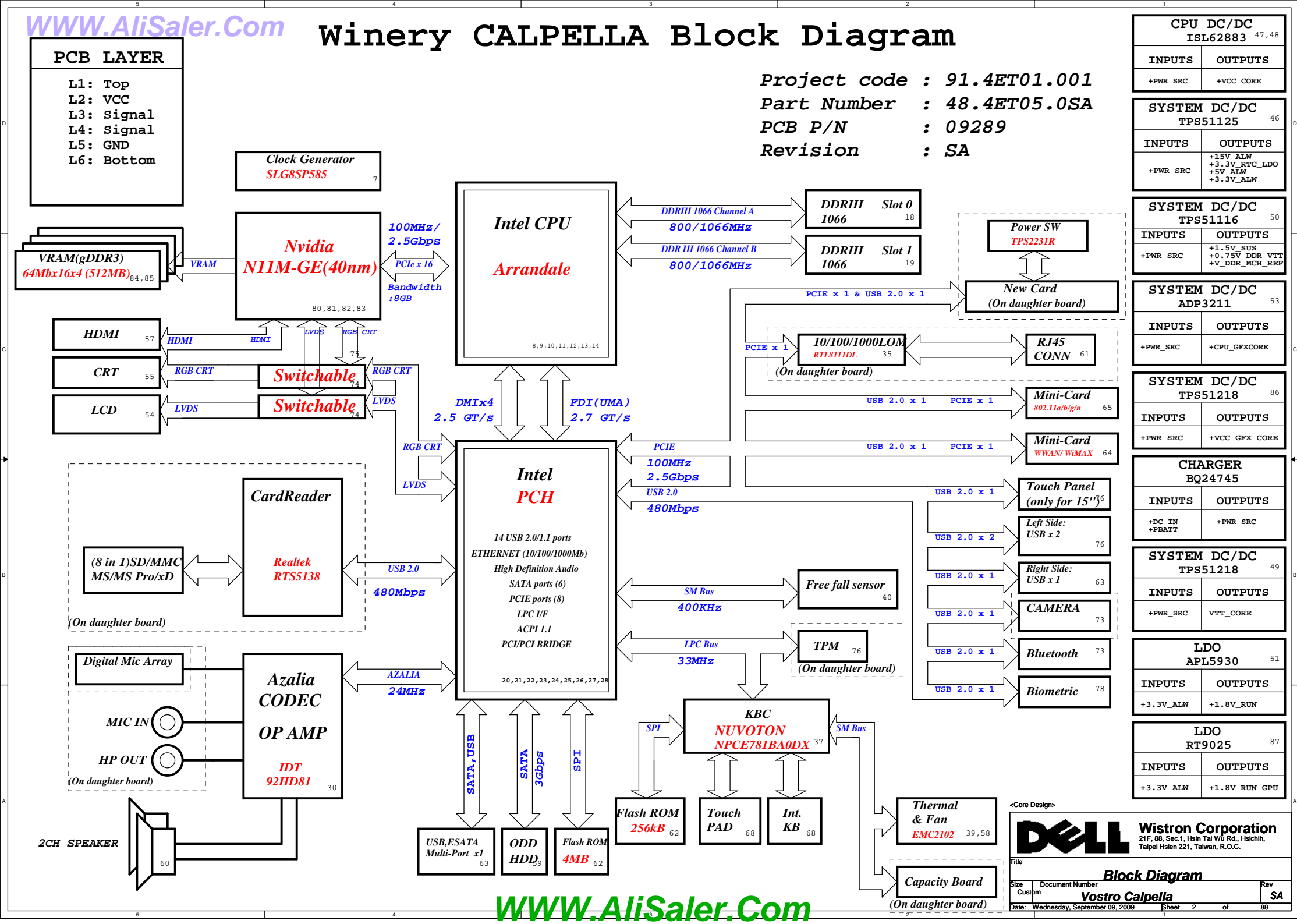
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L2: VCC  
L3: Signal  
L4: Signal  
L5: GND  
L6: Bottom

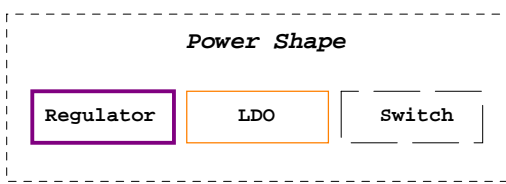
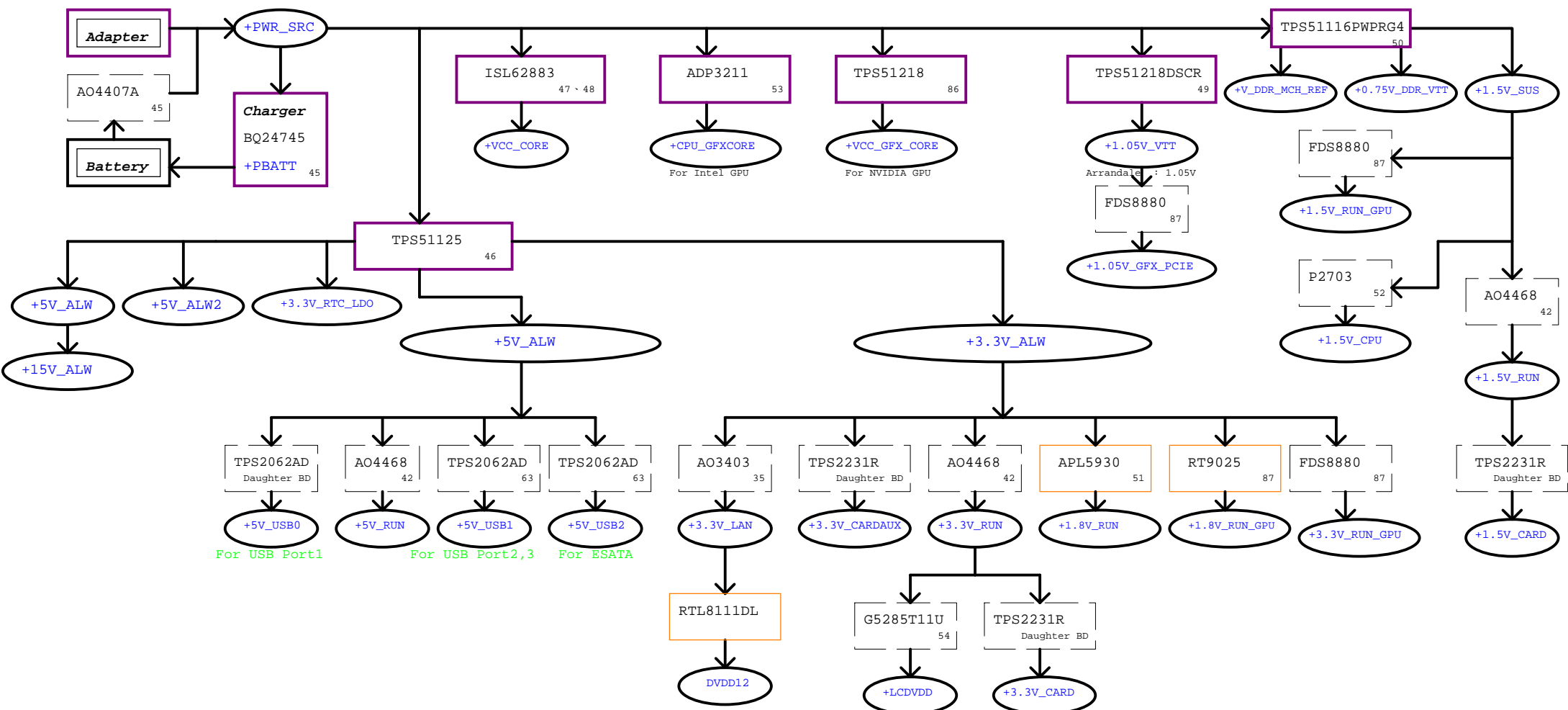
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Part Number : 48.4ET05.0SA

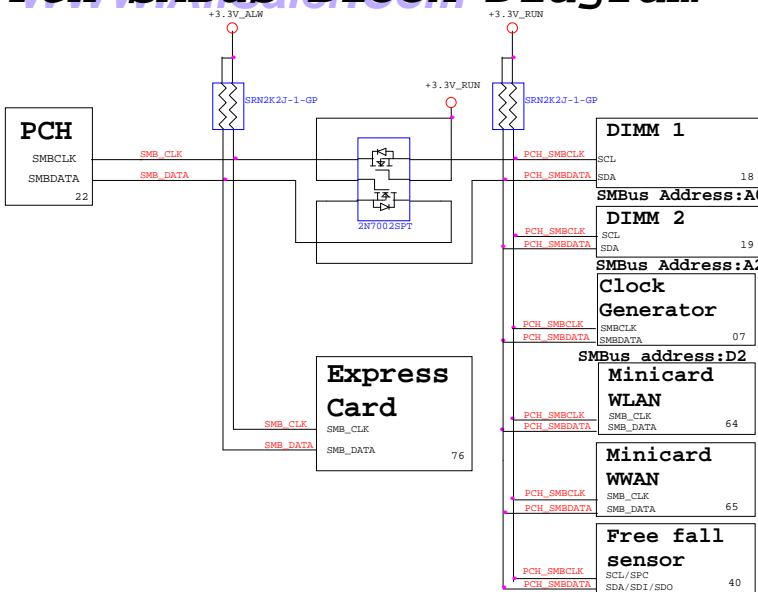
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Revision : SA

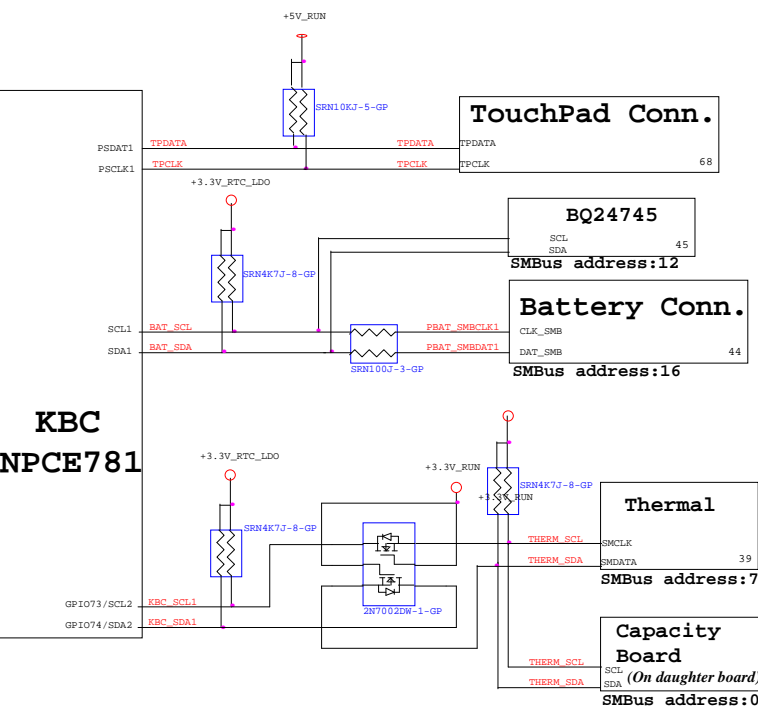




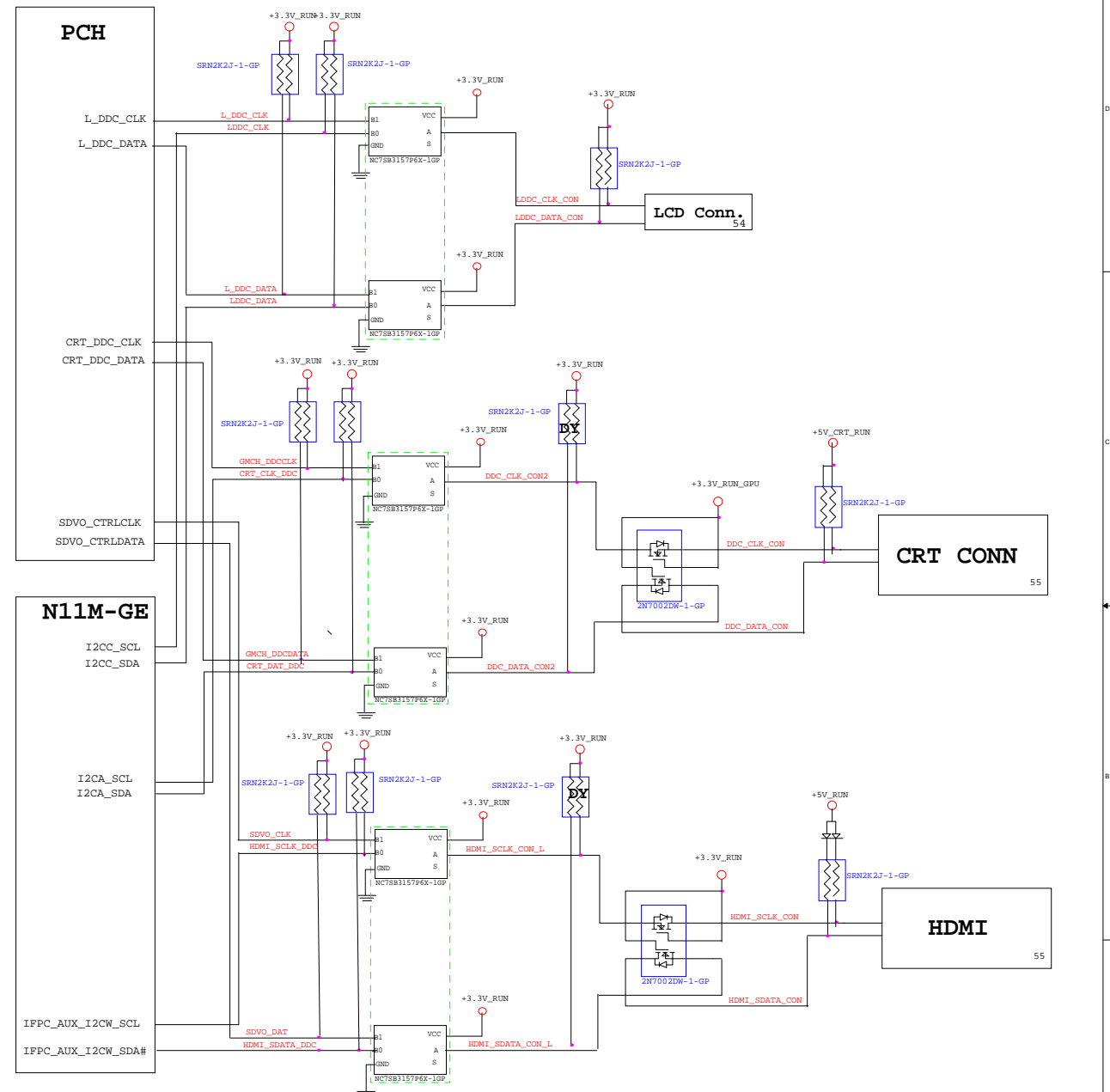
## PCH SMBus Block Diagram



### KBC SMBus Block Diagram



## Switchable Graphic SMBus Block Diagram



&lt;Core Design&gt;



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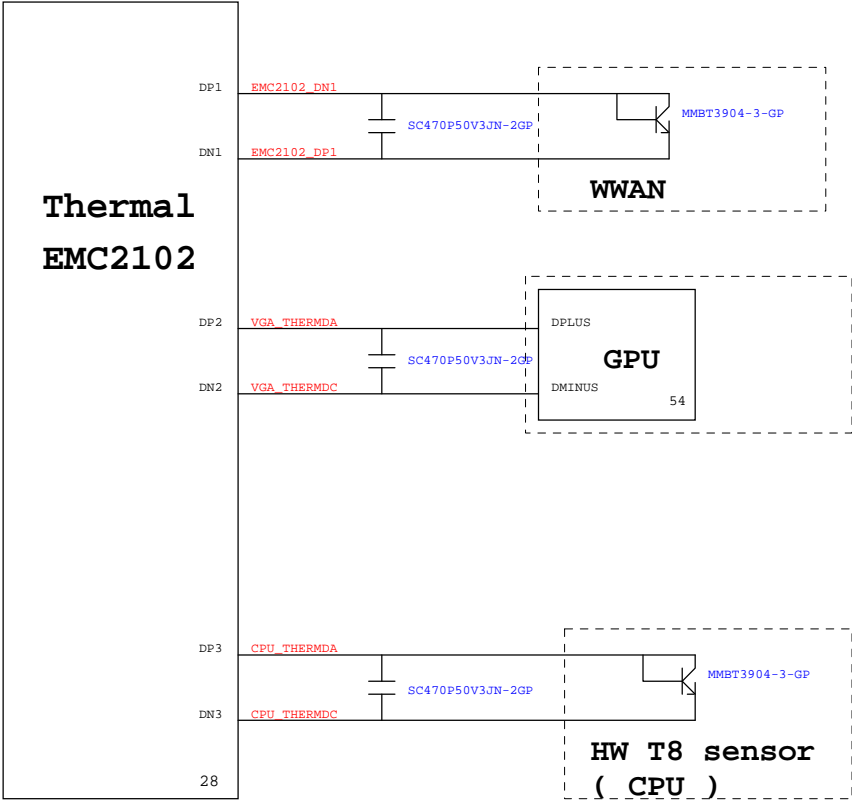
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### SMBUS Block Diagram

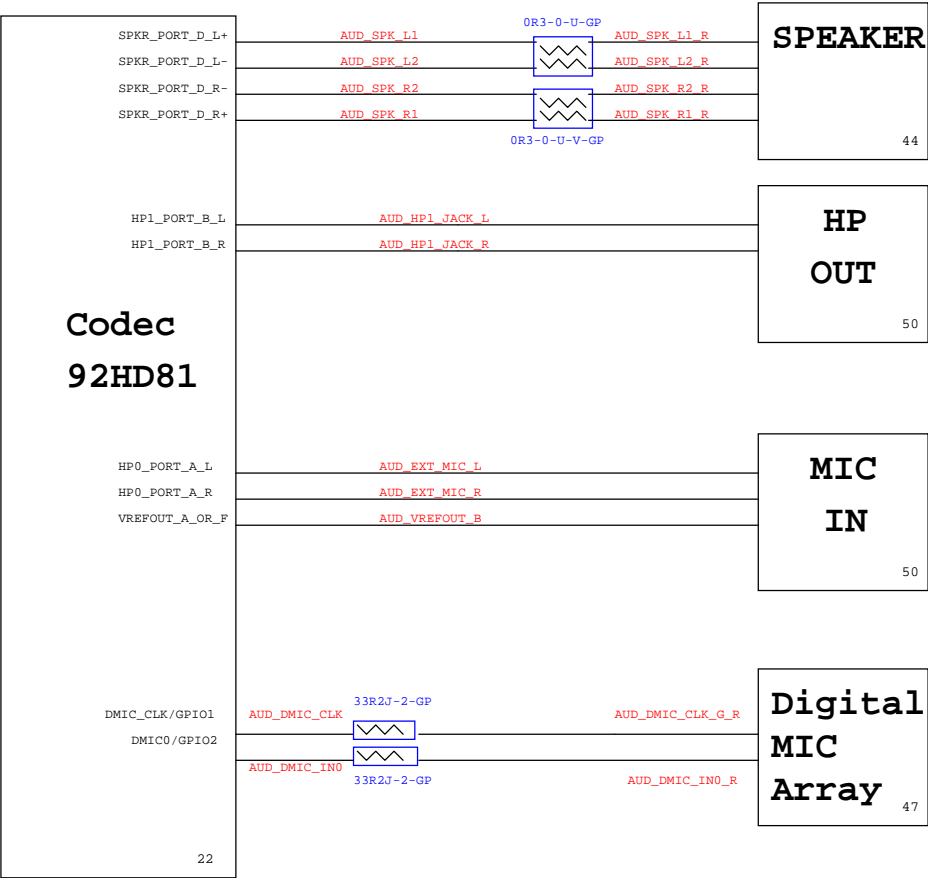
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C	<b>Vostro Calpella</b>	<b>SA</b>

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# Thermal Block Diagram



# Audio Block Diagram



Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap ModeNote: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 k do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing


LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

Processor Strapping

Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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Title

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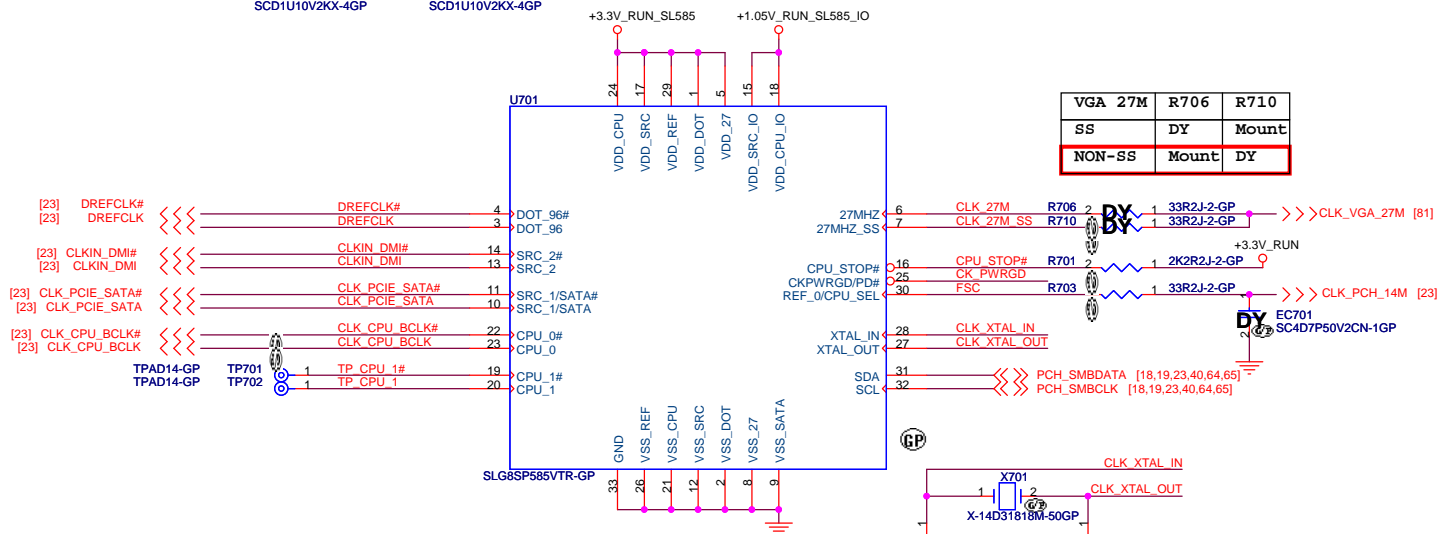
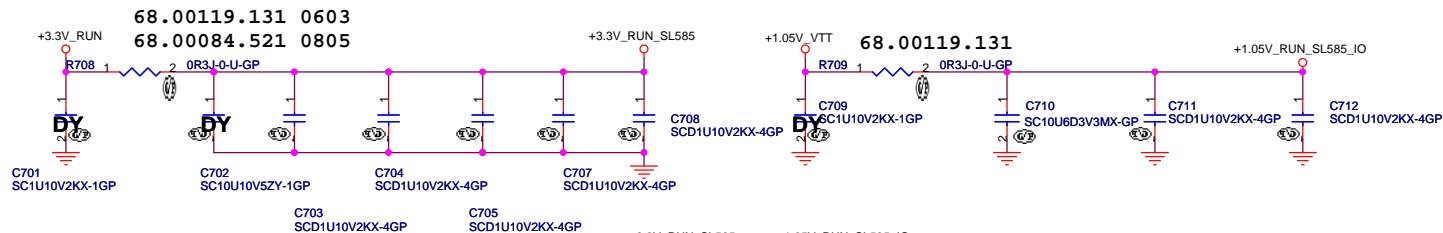
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Vostro Calpella

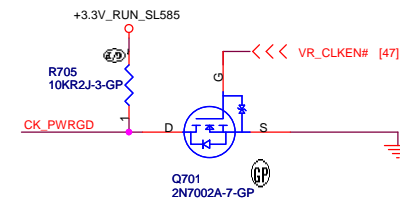
Rev  
SA

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VGA_27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY



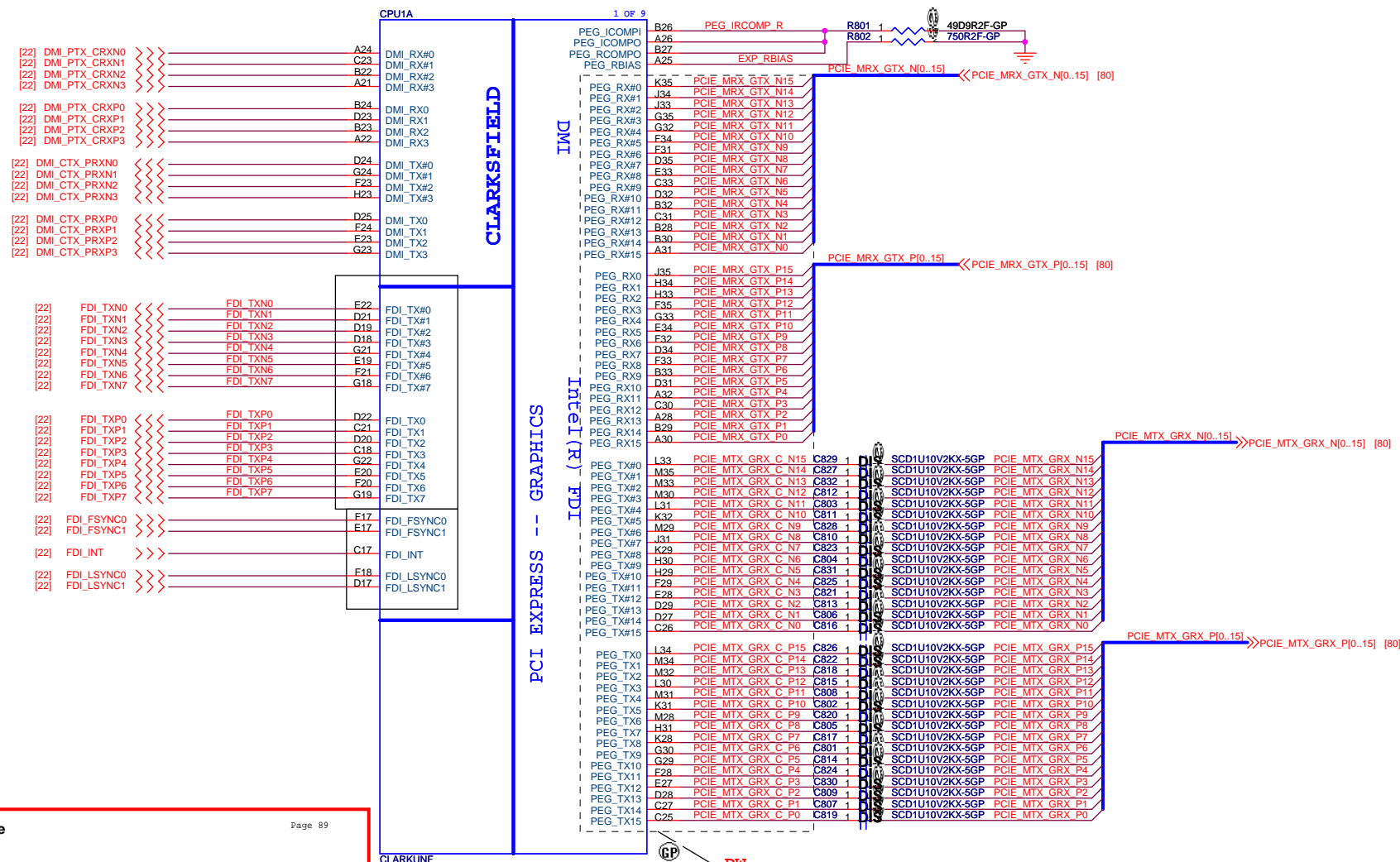
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2nd ICS 71.93197.003

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title	<b>Clock Generator SLG8SP585</b>		
Size	Document Number	Rev	X00
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**Calpella Platform Design Guide**  
**Revision 1.6**

## 2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI\_TX[7:0] and FDI\_TX#[7:0] can be left floating on the Arrandale. The GFX\_IMON, FDI\_FSYNC[0], FDI\_FSYNC[1], FDI\_LSYNC[0], FDI\_LSYNC[1], and FDI\_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

DW

07/02 Added  
1.Added Flexible Display Interface (IntelR FDI) commentariat

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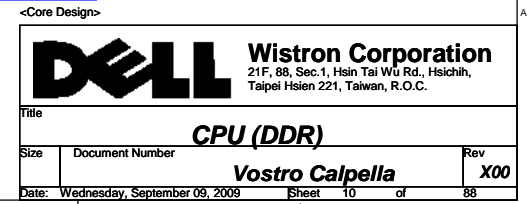


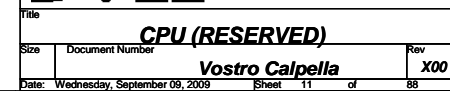
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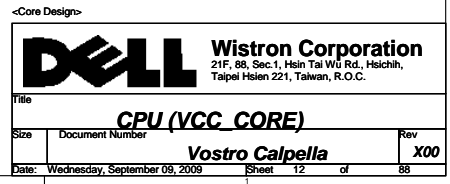
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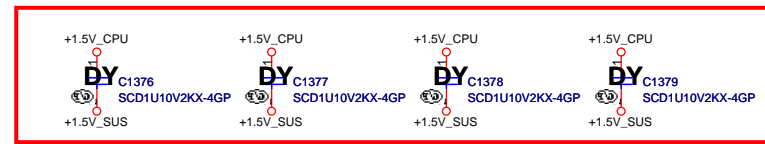
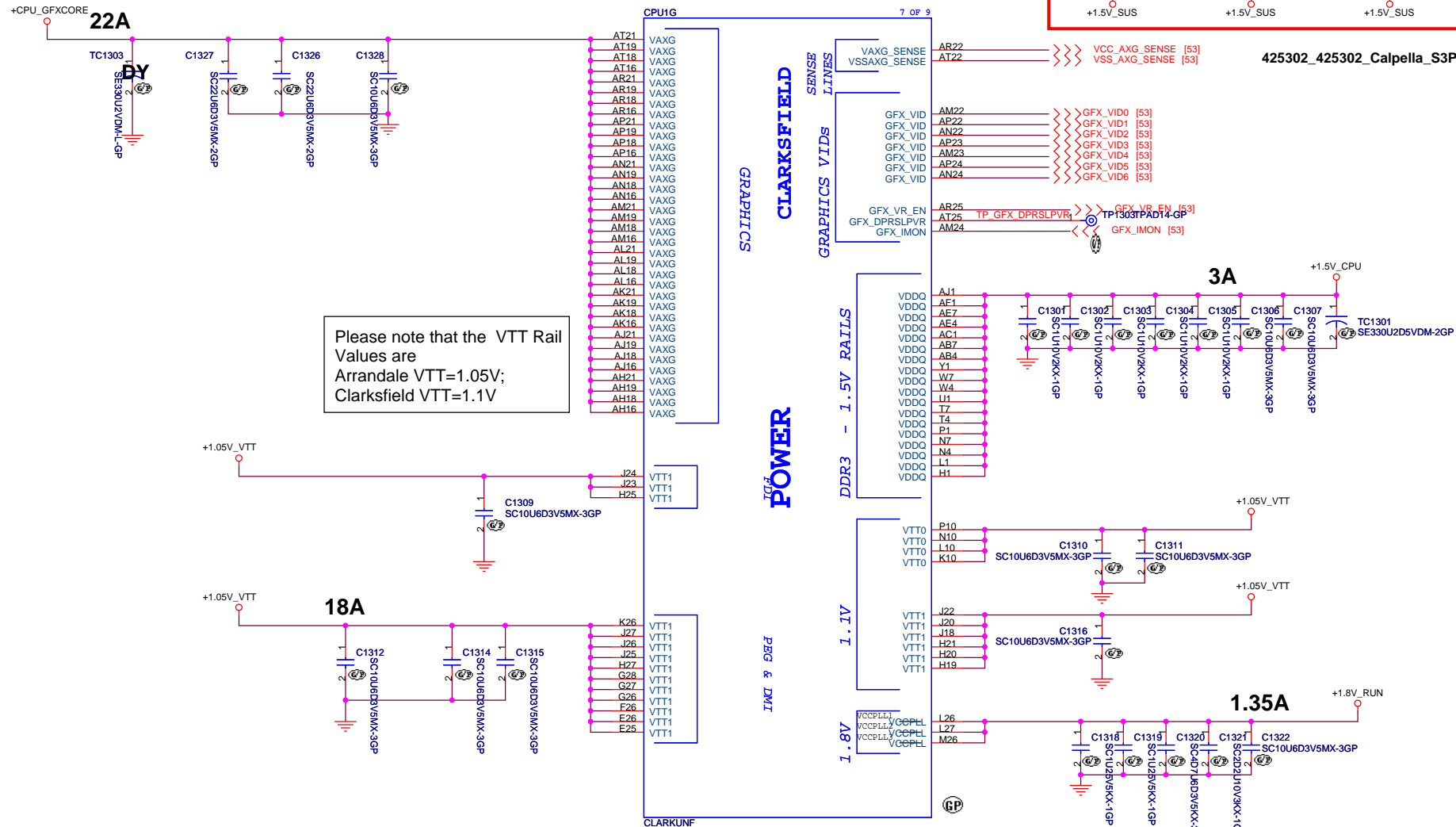












425302\_425302\_Calpella\_S3PowerReduction\_WhitePape  
Revision 0.7

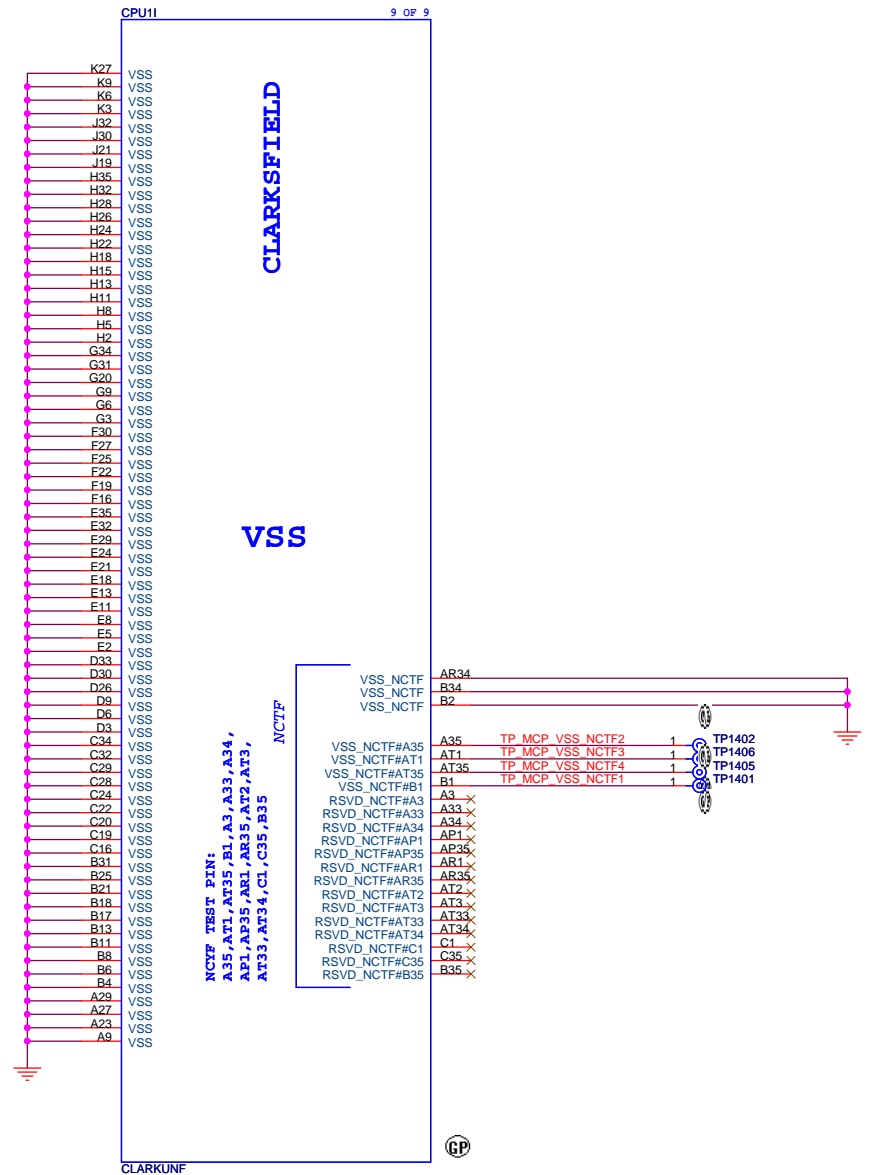
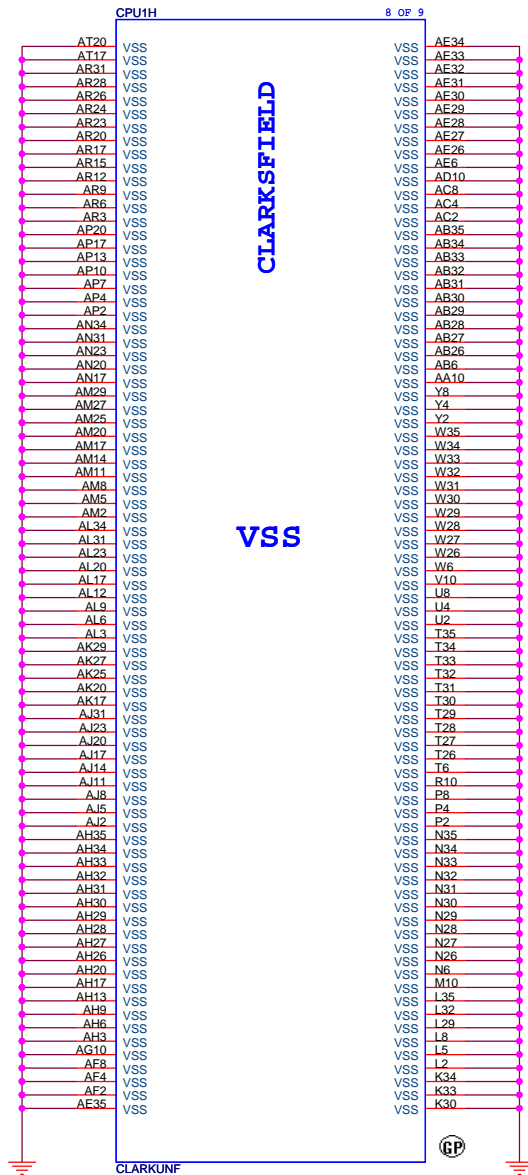
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Date: Wednesday, September 09, 2009 Sheet 13 of 88



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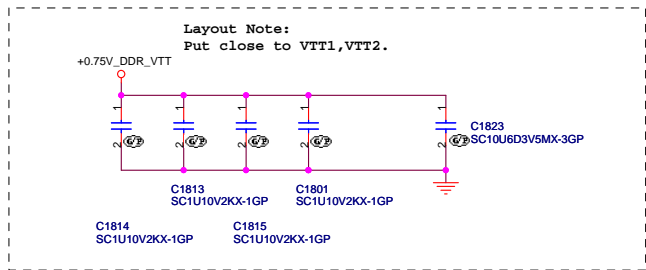
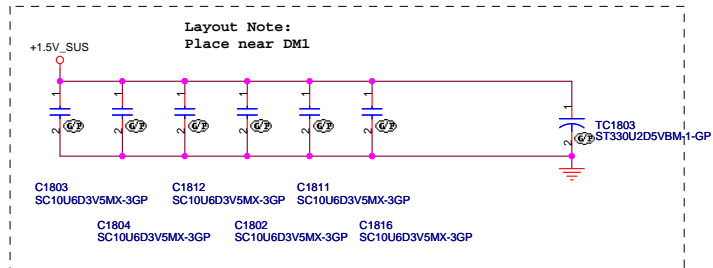
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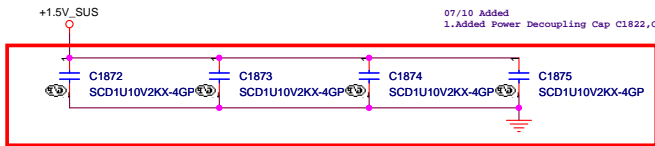
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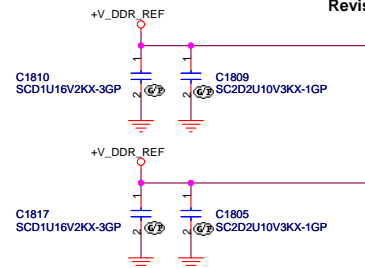
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DW  
07/10 Added  
1.Added Power Decoupling Cap C1822,C1823 Bason on design guide



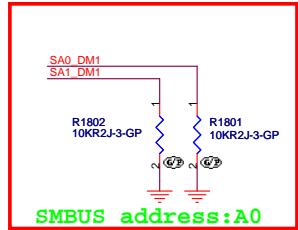
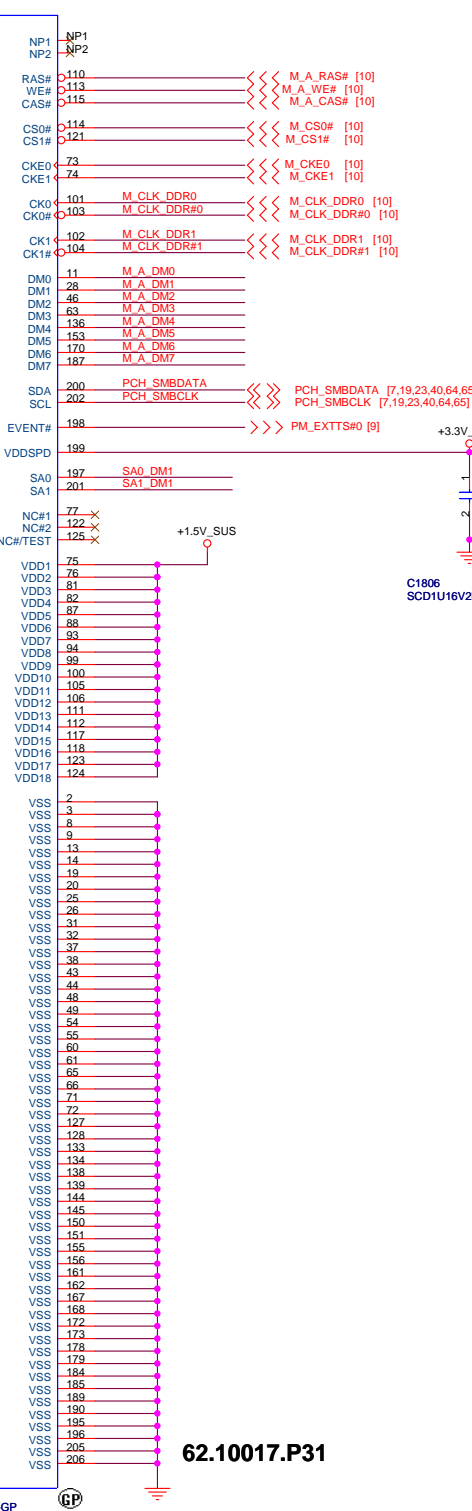
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Revision 0.7



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M_A A1	97	A1
M_A A2	96	A2
M_A A3	95	A3
M_A A4	92	A4
M_A A5	91	A5
M_A A6	90	A6
M_A A7	86	A7
M_A A8	89	A8
M_A A9	85	A9
M_A A10	107	A10/AP
M_A A11	84	A11
M_A A12	83	A12
M_A A13	119	A13
M_A A14	80	A14
M_A A15	78	A15
M_A BS2	79	A16/BA2
M_A BS0	109	BA0
M_A BS1	108	BA1
M_A DQ0	5	DQ0
M_A DQ1	7	DQ1
M_A DQ2	15	DQ2
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M_A DQ58	181	DQ58
M_A DQ59	193	DQ59
M_A DQ60	180	DQ60
M_A DQ61	182	DQ61
M_A DQ62	192	DQ62
M_A DQ63	194	DQ63
M_A DQS#0	10	DQS0#
M_A DQS#1	27	DQS1#
M_A DQS#2	45	DQS2#
M_A DQS#3	62	DQS3#
M_A DQS#4	135	DQS4#
M_A DQS#5	152	DQS5#
M_A DQS#6	169	DQS6#
M_A DQS#7	186	DQS7#
M_A DQS0	12	DQS0
M_A DQS1	29	DQS1
M_A DQS2	47	DQS2
M_A DQS3	64	DQS3
M_A DQS4	137	DQS4
M_A DQS5	154	DQS5
M_A DQS6	171	DQS6
M_A DQS7	188	DQS7

Height 5.2mm



DW  
07/02 Reserve  
1.Added SA0\_DM1 pull-up resistor  
07/07  
2.Reserve pull-hi,lo resistor

C1806  
SCD1U16V2KX-3GP  
C1807  
SCD2U10V3KX-1GP

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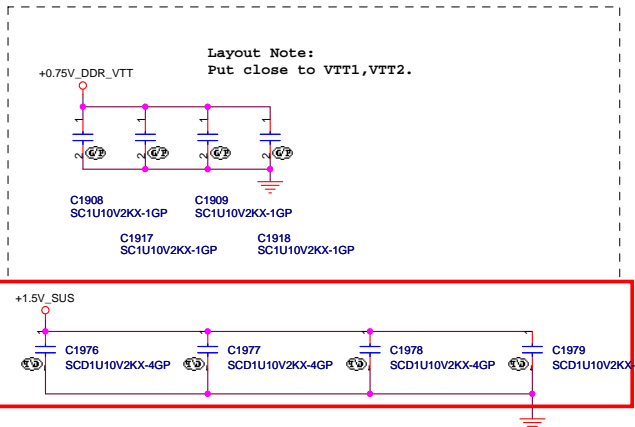
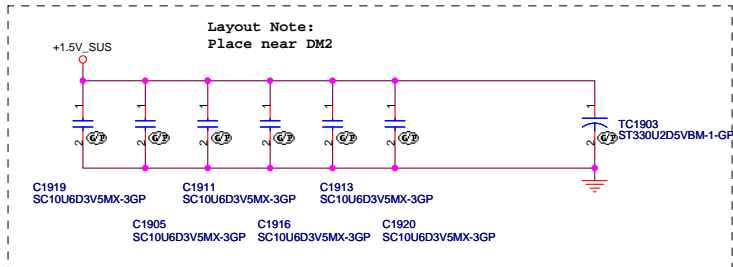
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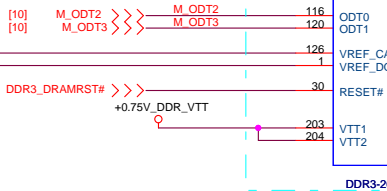
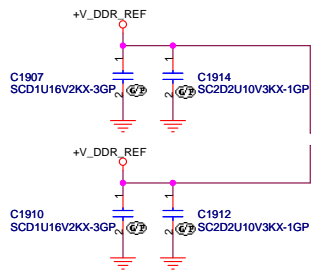
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Revision 0.7

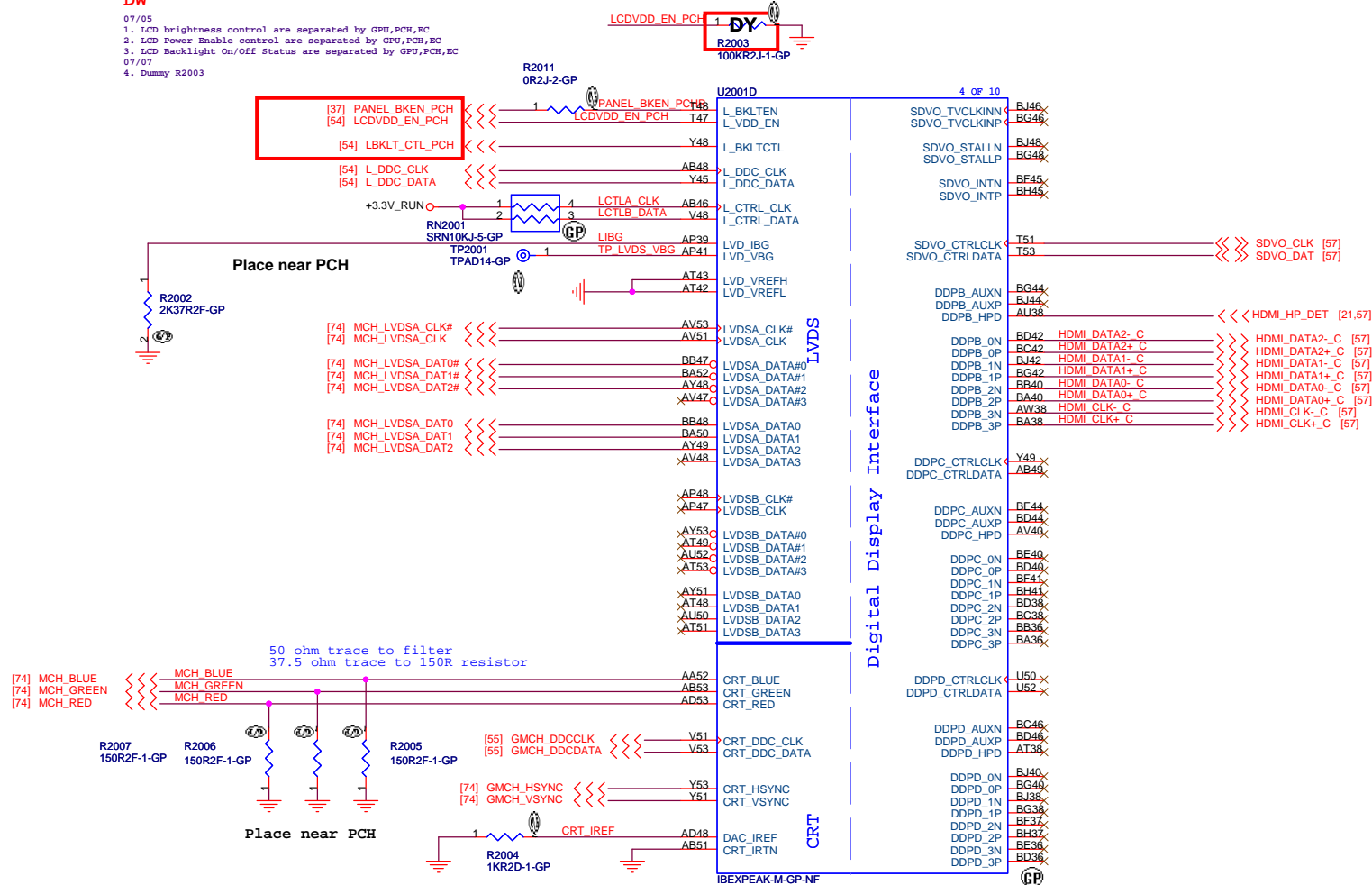


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M_B A1	97	A1	NP2	NP2	NP2	NP2
M_B A2	96	A2	RAS#	WE#	CAS#	CAS#
M_B A3	95	A3	CS0#	CS1#	CS2#	CS3#
M_B A4	94	A4	CKE0	CKE1	CKE2	CKE3
M_B A5	93	A5	CK0#	CK1#	CK2#	CK3#
M_B A6	92	A6	DM0	DM1	DM2	DM3
M_B A7	91	A7	DM4	DM5	DM6	DM7
M_B A8	90	A8	DM8	DM9	DM10	DM11
M_B A9	89	A9	DM12	DM13	DM14	DM15
M_B A10	88	A10	DM16	DM17	DM18	DM19
M_B A11	87	A11	DM20	DM21	DM22	DM23
M_B A12	86	A12	DM24	DM25	DM26	DM27
M_B A13	85	A13	DM28	DM29	DM30	DM31
M_B A14	84	A14	DM32	DM33	DM34	DM35
M_B A15	83	A15	DM36	DM37	DM38	DM39
M_B BS2	79	BA2	DM40	DM41	DM42	DM43
M_B BS0	109	BA0	DM44	DM45	DM46	DM47
M_B BS1	108	BA1	DM48	DM49	DM50	DM51
M_B DQ0	5	DQ0	DM52	DM53	DM54	DM55
M_B DQ1	6	DQ1	DM56	DM57	DM58	DM59
M_B DQ2	15	DQ2	DM60	DM61	DM62	DM63
M_B DQ3	17	DQ3	DM64	DM65	DM66	DM67
M_B DQ4	4	DQ4	DM68	DM69	DM70	DM71
M_B DQ5	16	DQ5	DM72	DM73	DM74	DM75
M_B DQ6	18	DQ6	DM76	DM77	DM78	DM79
M_B DQ7	21	DQ7	DM80	DM81	DM82	DM83
M_B DQ8	23	DQ8	DM84	DM85	DM86	DM87
M_B DQ9	33	DQ9	DM88	DM89	DM90	DM91
M_B DQ10	35	DQ10	DM92	DM93	DM94	DM95
M_B DQ11	36	DQ11	DM96	DM97	DM98	DM99
M_B DQ12	24	DQ12	DM100	DM101	DM102	DM103
M_B DQ13	34	DQ13	DM104	DM105	DM106	DM107
M_B DQ14	36	DQ14	DM108	DM109	DM110	DM111
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M_B DQ36	132	DQ36	DM196	DM197	DM198	DM199
M_B DQ37	140	DQ37	DM200	DM201	DM202	DM203
M_B DQ38	142	DQ38	DM204	DM205	DM206	DM207
M_B DQ39	147	DQ39	DM208	DM209	DM210	DM211
M_B DQ40	149	DQ40	DM212	DM213	DM214	DM215
M_B DQ41	157	DQ41	DM216	DM217	DM218	DM219
M_B DQ42	159	DQ42	DM220	DM221	DM222	DM223
M_B DQ43	146	DQ43	DM224	DM225	DM226	DM227
M_B DQ44	148	DQ44	DM228	DM229	DM230	DM231
M_B DQ45	158	DQ45	DM232	DM233	DM234	DM235
M_B DQ46	160	DQ46	DM236	DM237	DM238	DM239
M_B DQ47	163	DQ47	DM240	DM241	DM242	DM243
M_B DQ48	175	DQ48	DM244	DM245	DM246	DM247
M_B DQ49	177	DQ49	DM248	DM249	DM250	DM251
M_B DQ50	164	DQ50	DM252	DM253	DM254	DM255
M_B DQ51	166	DQ51	DM256	DM257	DM258	DM259
M_B DQ52	174	DQ52	DM260	DM261	DM262	DM263
M_B DQ53	176	DQ53	DM264	DM265	DM266	DM267
M_B DQ54	181	DQ54	DM268	DM269	DM270	DM271
M_B DQ55	183	DQ55	DM272	DM273	DM274	DM275
M_B DQ56	191	DQ56	DM276	DM277	DM278	DM279
M_B DQ57	193	DQ57	DM280	DM281	DM282	DM283
M_B DQ58	180	DQ58	DM284	DM285	DM286	DM287
M_B DQ59	182	DQ59	DM288	DM289	DM290	DM291
M_B DQ60	192	DQ60	DM292	DM293	DM294	DM295
M_B DQ61	194	DQ61	DM296	DM297	DM298	DM299
M_B DQ62	10	DQ62	DM300	DM301	DM302	DM303
M_B DQ63	21	DQ63	DM304	DM305	DM306	DM307
M_B DQS#0	22	DQS0	DM308	DM309	DM310	DM311
M_B DQS#1	45	DQS1	DM312	DM313	DM314	DM315
M_B DQS#2	62	DQS2	DM316	DM317	DM318	DM319
M_B DQS#3	135	DQS3	DM320	DM321	DM322	DM323
M_B DQS#4	152	DQS4	DM324	DM325	DM326	DM327
M_B DQS#5	168	DQS5	DM328	DM329	DM330	DM331
M_B DQS#6	186	DQS6	DM332	DM333	DM334	DM335
M_B DQS#7	12	DQS7	DM336	DM337	DM338	DM339
M_B DQ50	29	DQ50	DM340	DM341	DM342	DM343
M_B DQ51	47	DQ51	DM344	DM345	DM346	DM347
M_B DQ52	64	DQ52	DM348	DM349	DM350	DM351
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M_B DQ54	154	DQ54	DM356	DM357	DM358	DM359
M_B DQ55	171	DQ55	DM360	DM361	DM362	DM363
M_B DQ56	188	DQ56	DM364	DM365	DM366	DM367
M_B DQ57	12	DQ57	DM368	DM369	DM370	DM371
M_B DQ58	29	DQ58	DM372	DM373	DM374	DM375
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M_B DQ61	137	DQ61	DM384	DM385	DM386	DM387
M_B DQ62	154	DQ62	DM388	DM389	DM390	DM391
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M_B DQ66	29	DQ66	DM404	DM405	DM406	DM407
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M_B DQ88	188	DQ88	DM492	DM493	DM494	DM495
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M_B DQ90	29	DQ90	DM500	DM501	DM502	DM503
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M_B DQ130	29	DQ130	DM660	DM661	DM662	DM663
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M_B DQ133	137	DQ133	DM672	DM673	DM674	DM675
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DW

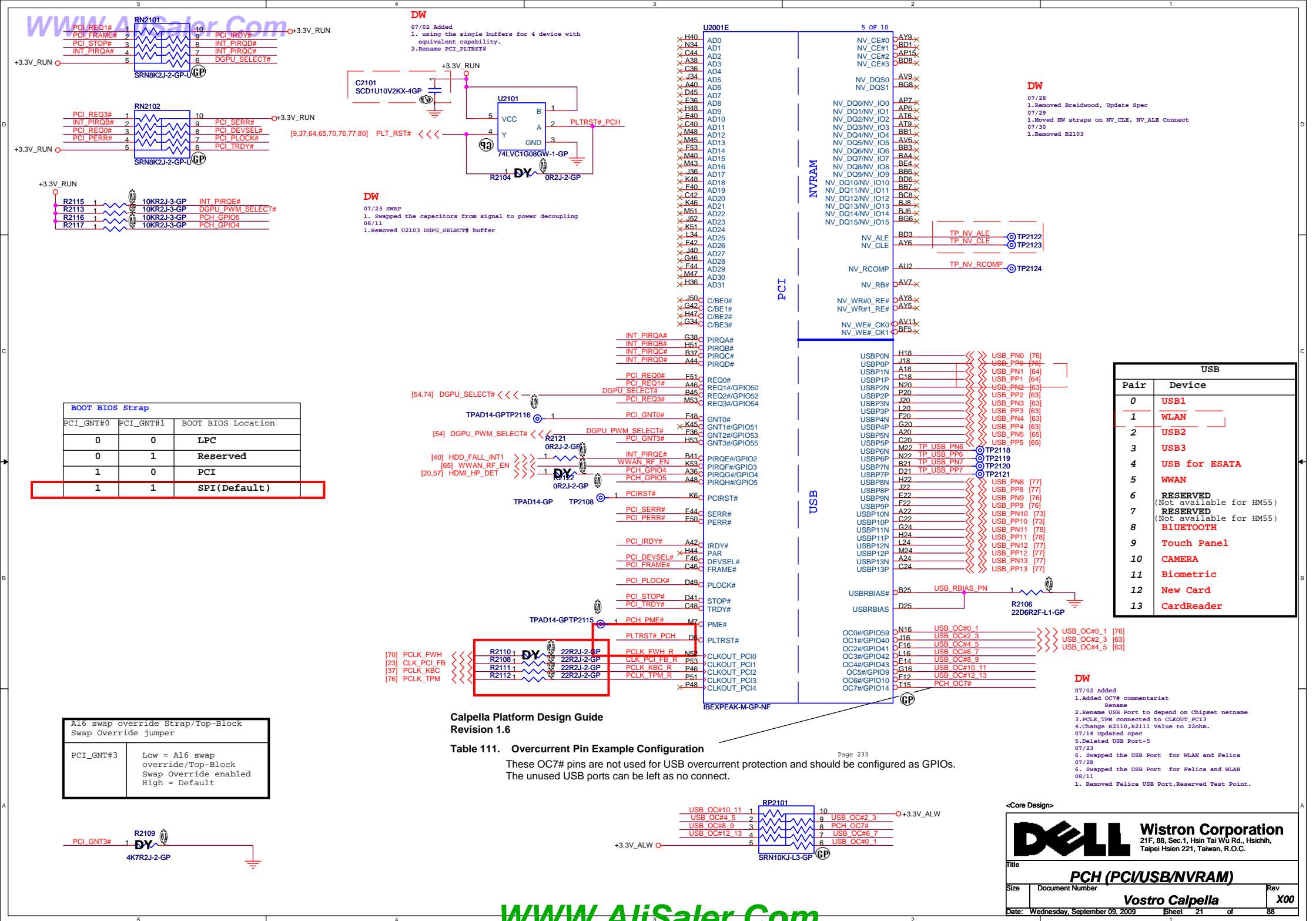
07/05

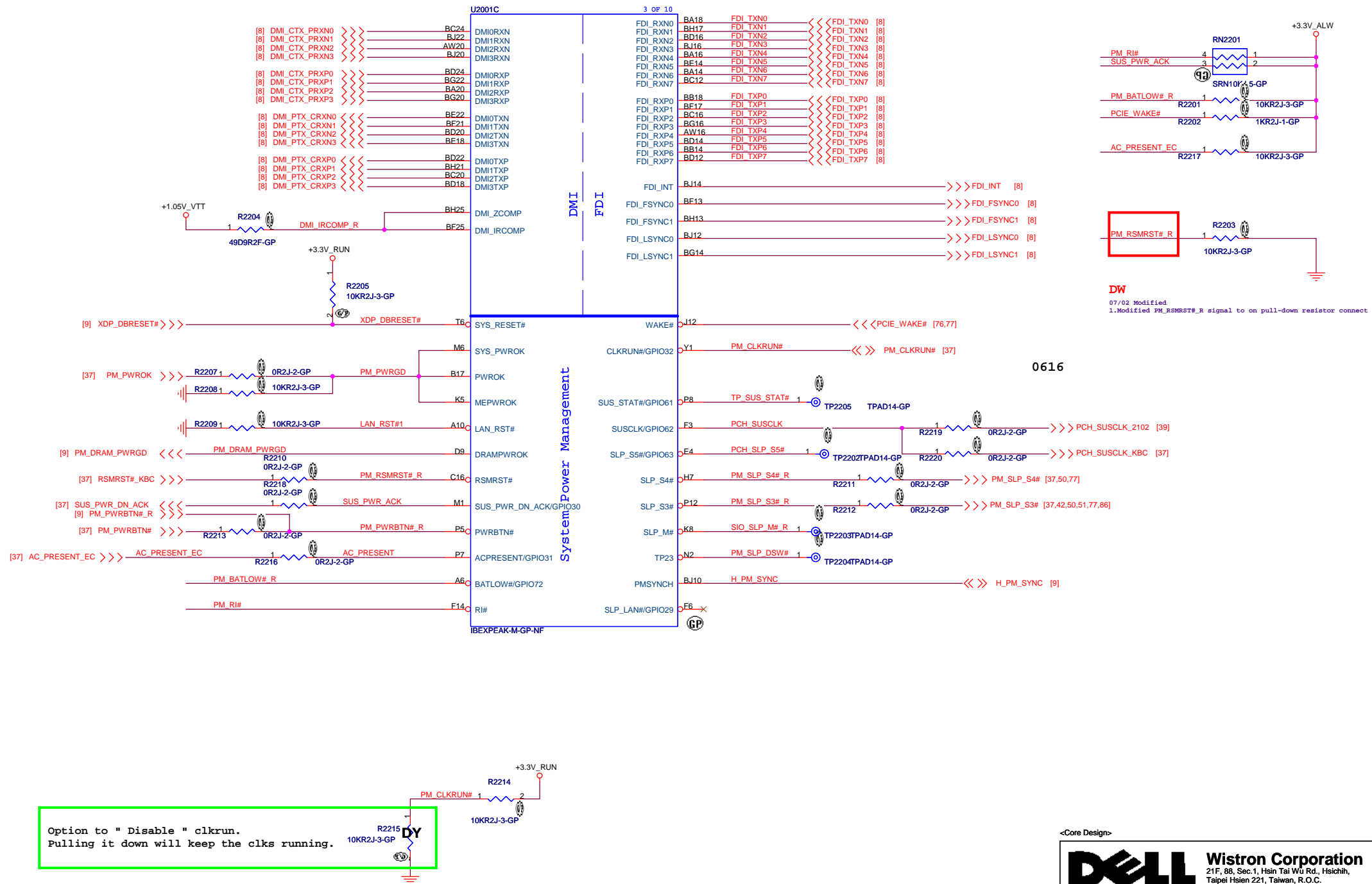
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
- 07/07
4. Dummy R2003

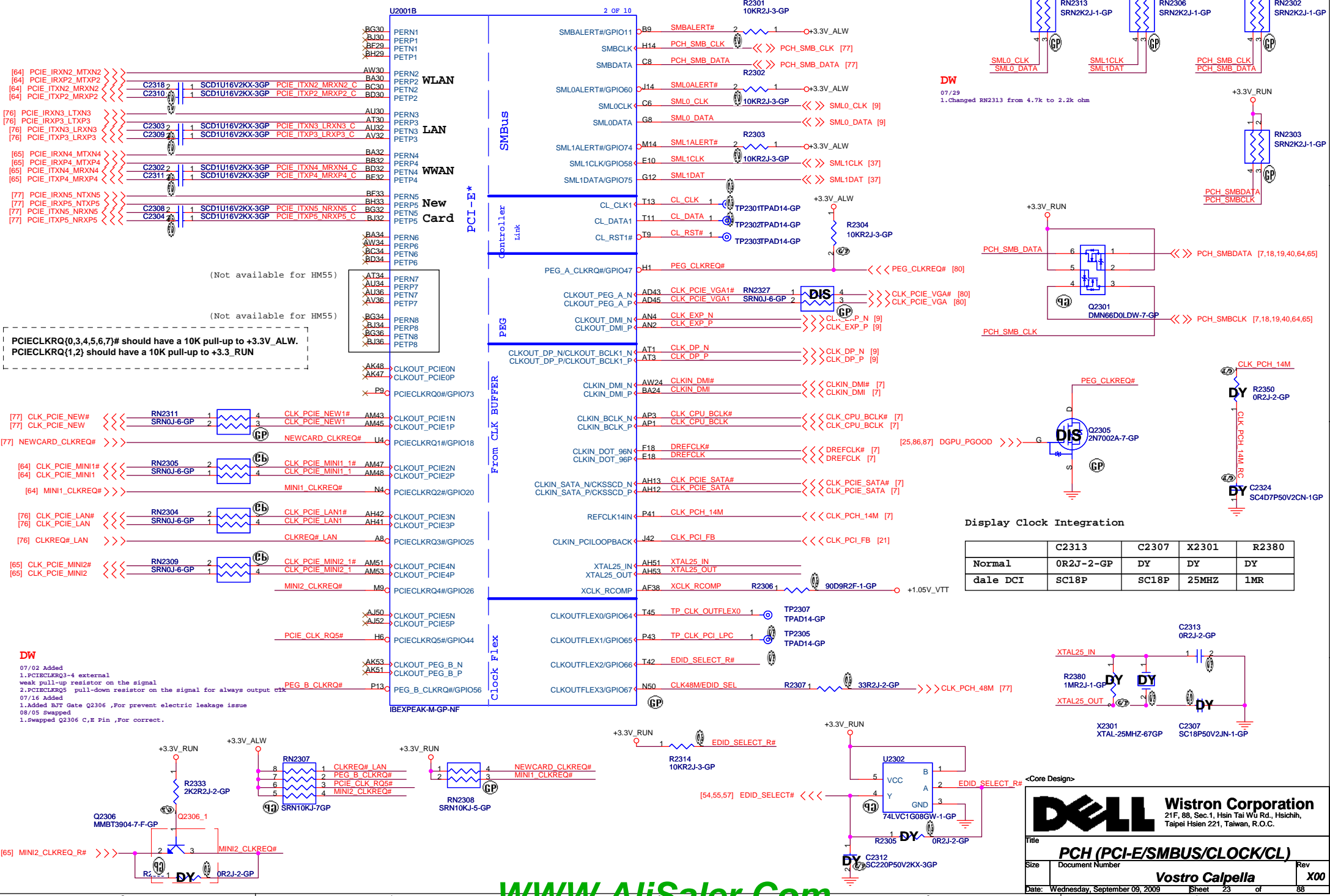


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		Title: <b>PCH (LVDS/CRT/DDI)</b>	
Size	Document Number	Rev	X00
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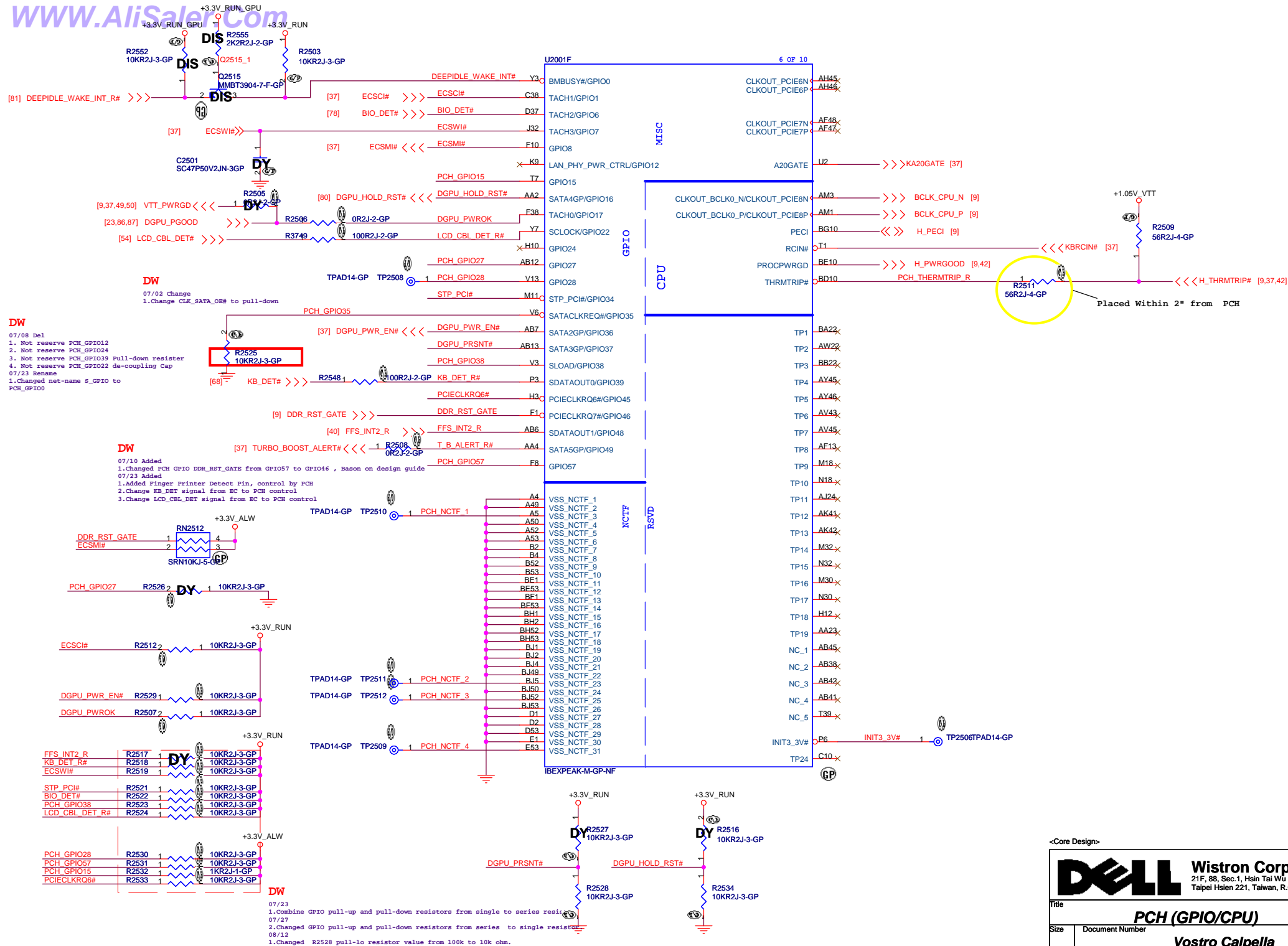


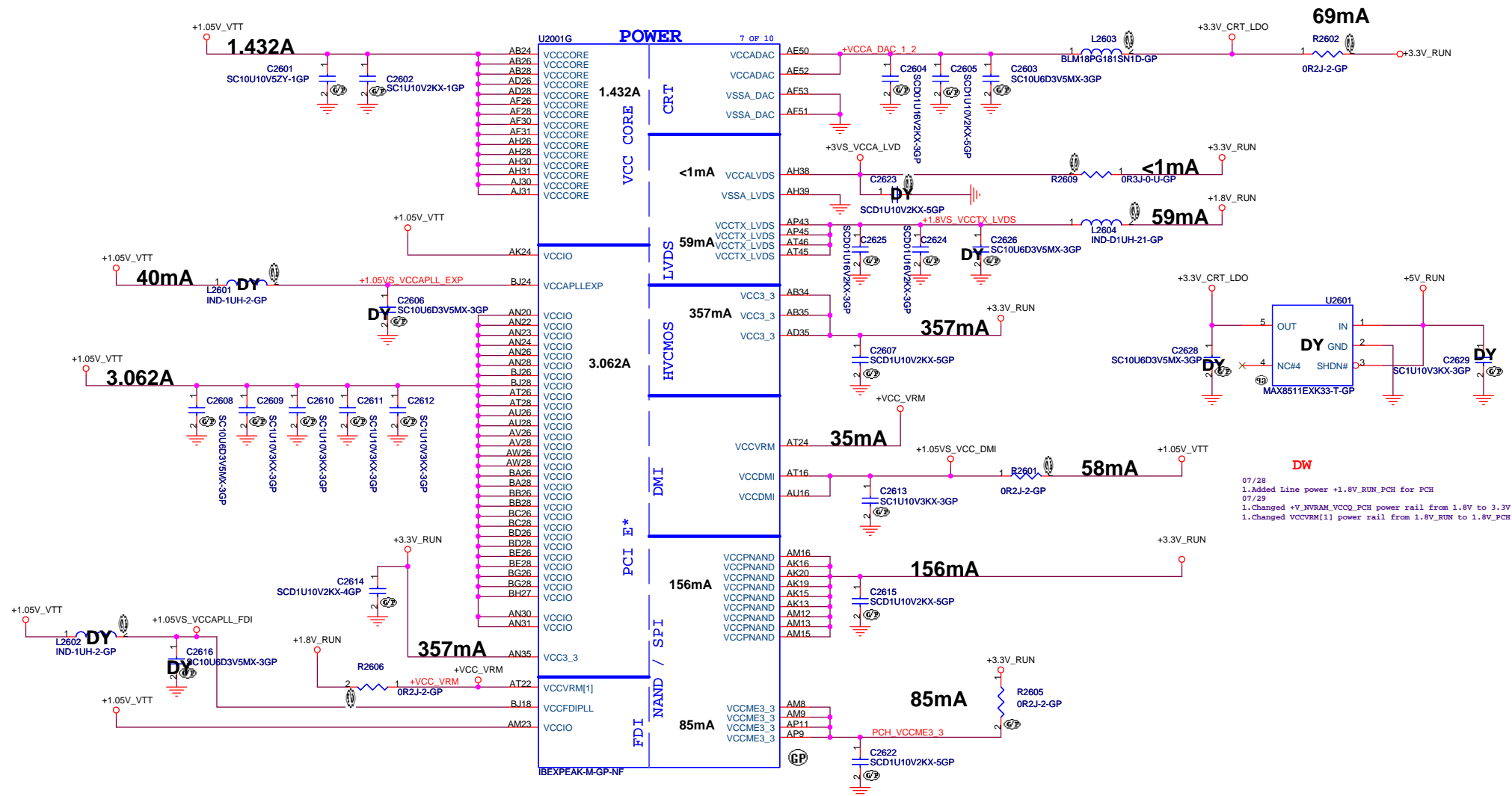












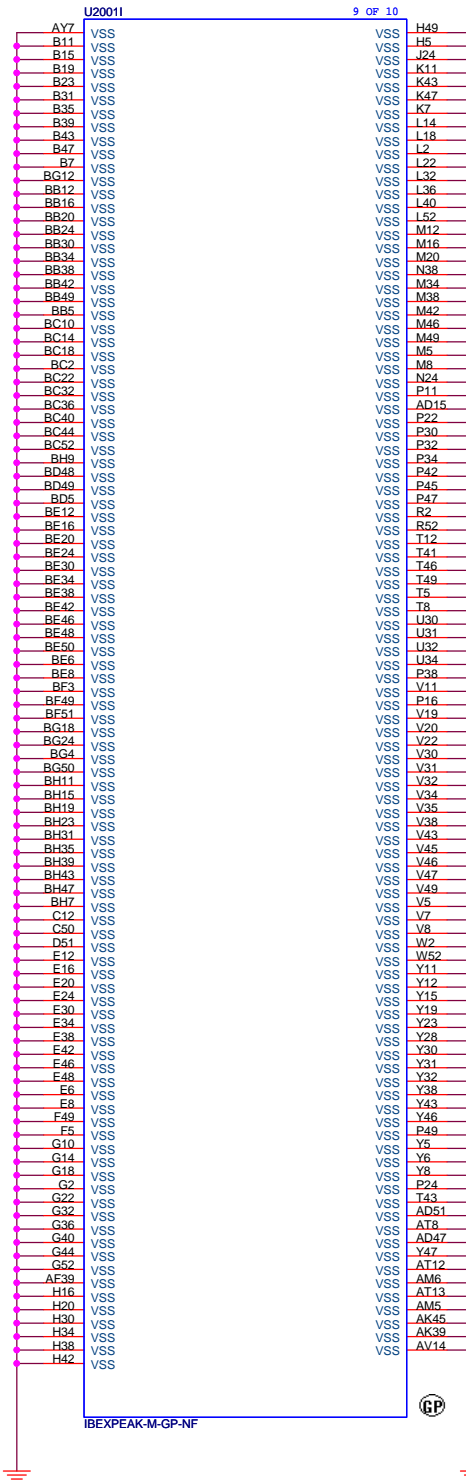
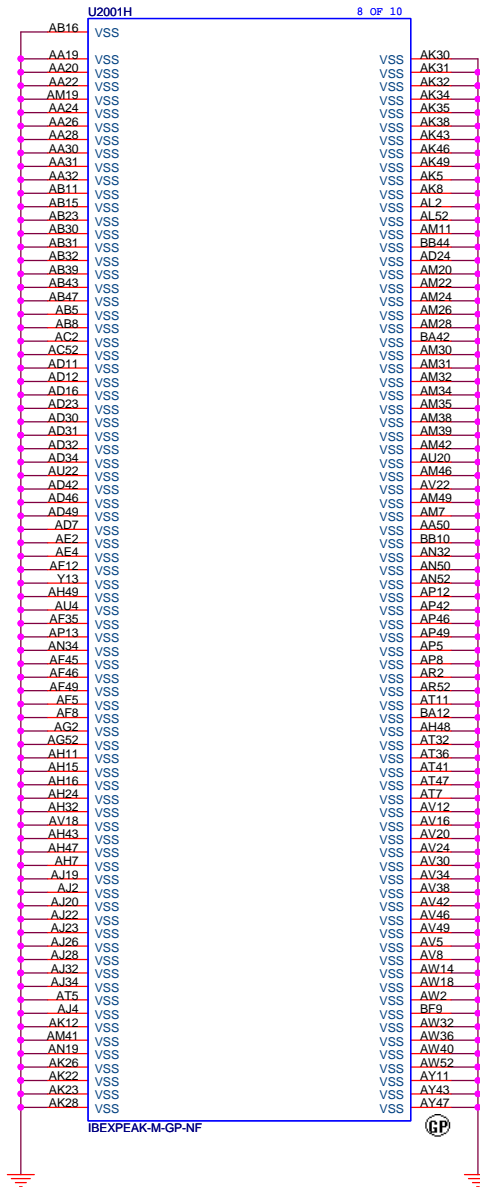
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Title				
<b>PCH (POWER1)</b>				
Size	Document Number			Rev
<b>Vostro Calpella</b>			<b>X00</b>	
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Document Number

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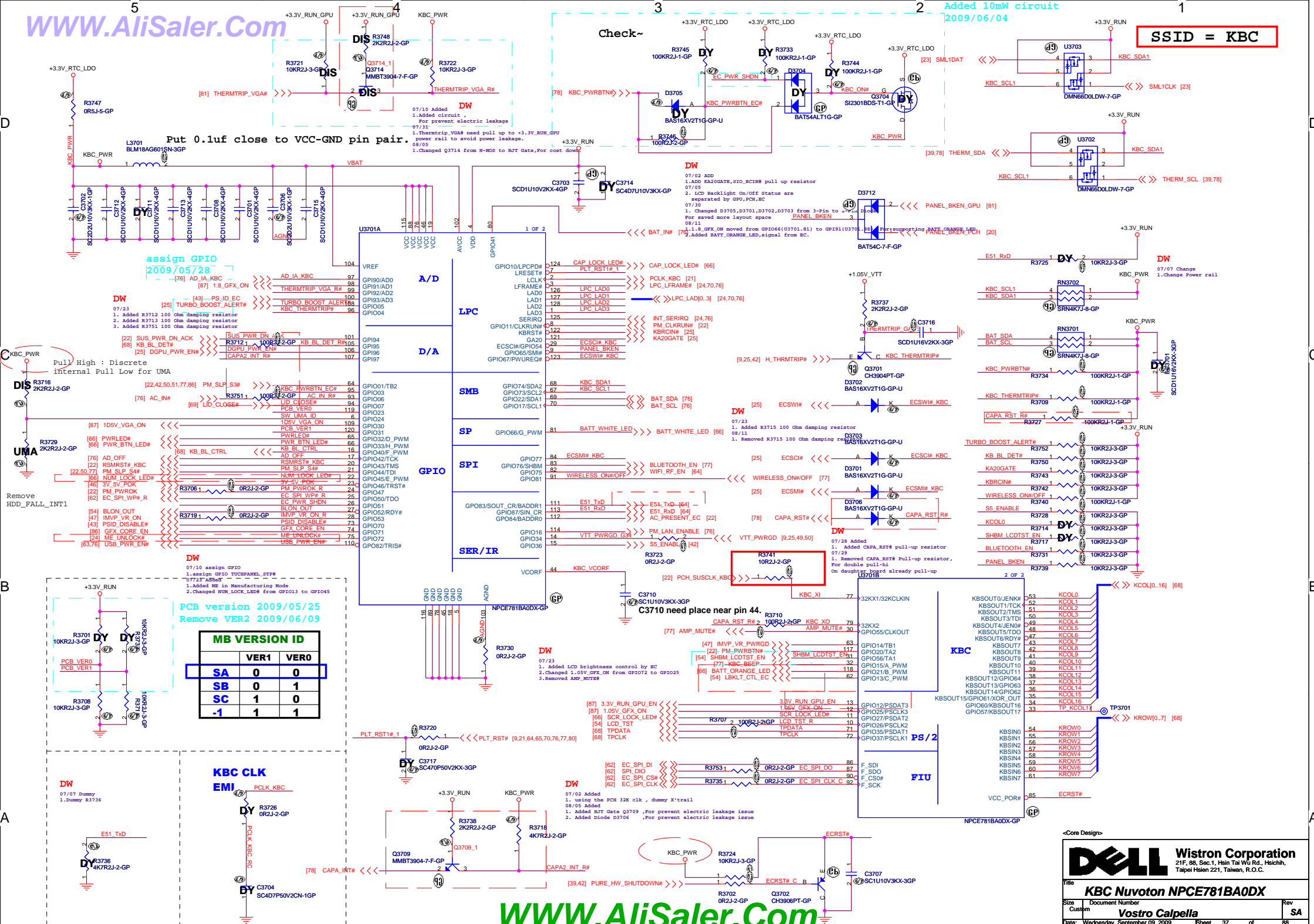
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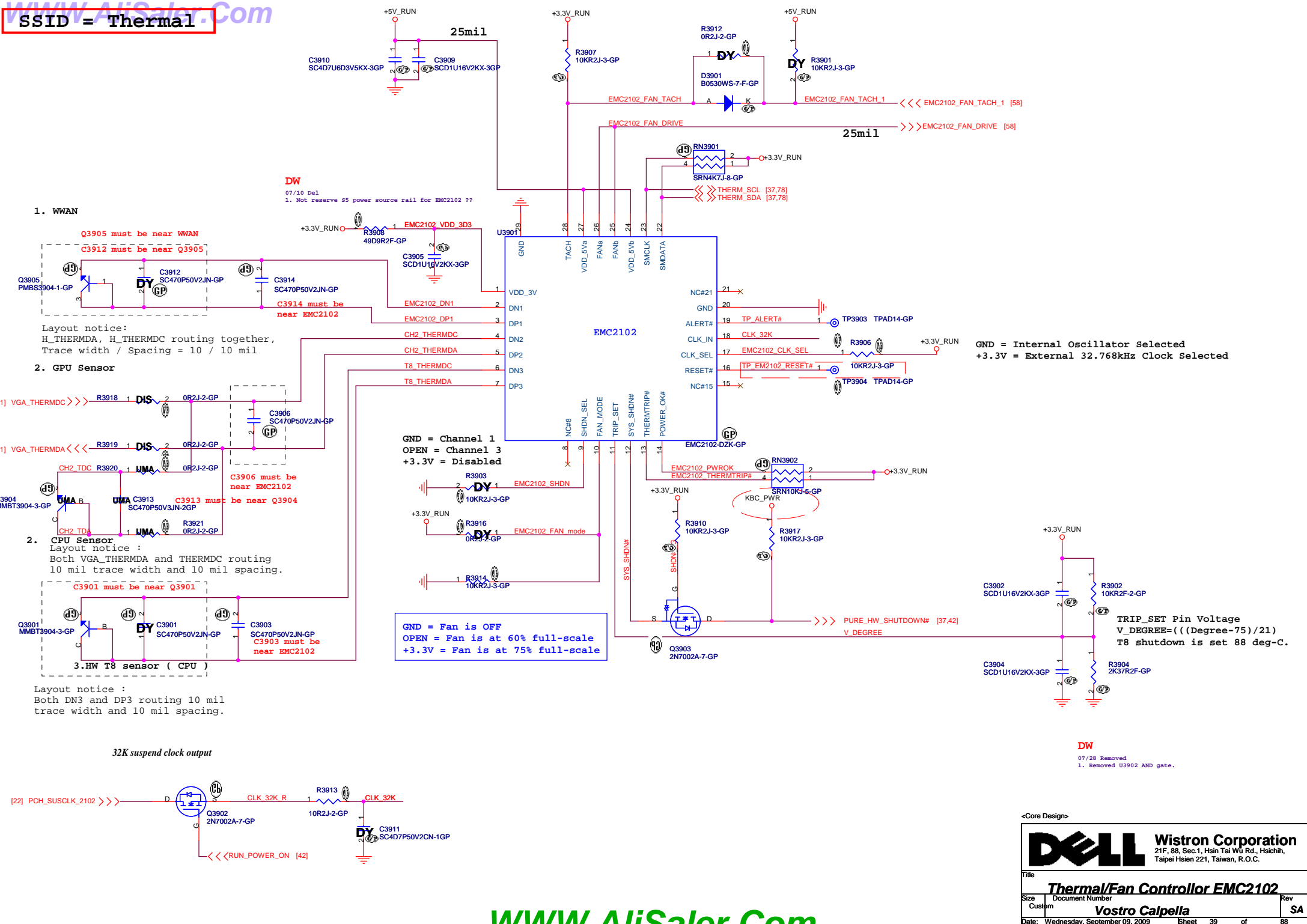
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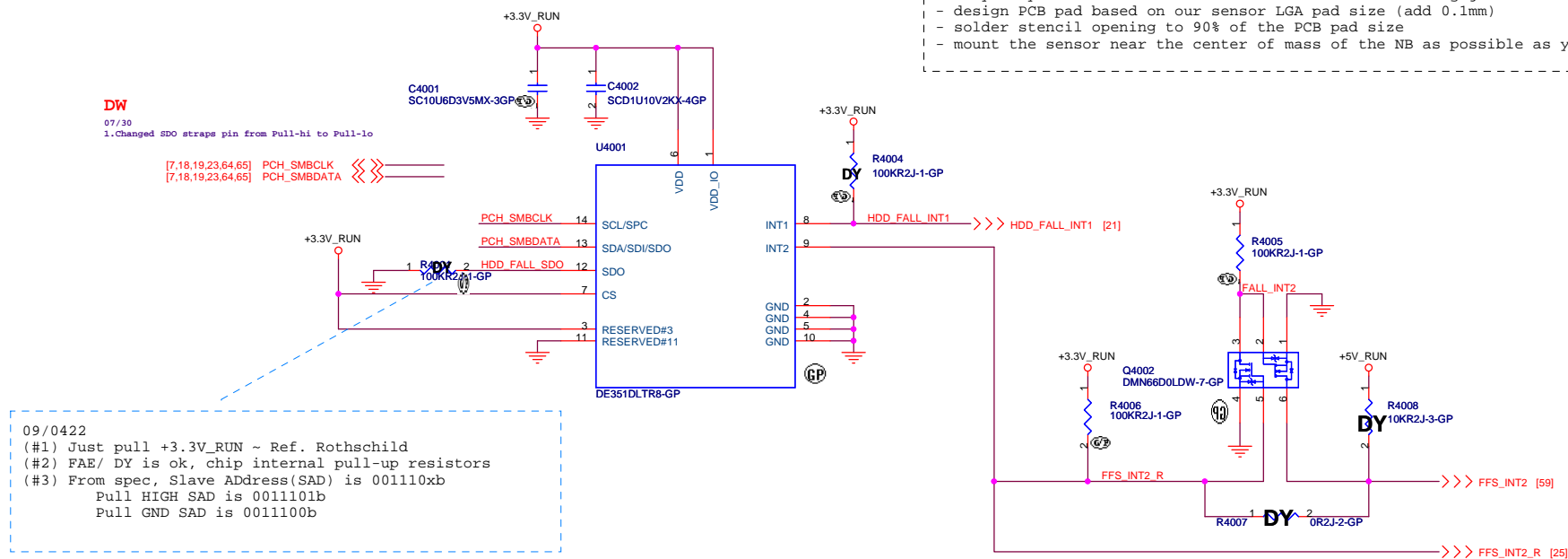
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SSID = User.Interface

## Free Fall Sensor



Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of the mass of the NB as possible as you can

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

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Title			
<b>Free Fall Sensor</b>			
Size	Document Number	Rev	
Custom	<b>Vostro Calpella</b>	<b>SA</b>	
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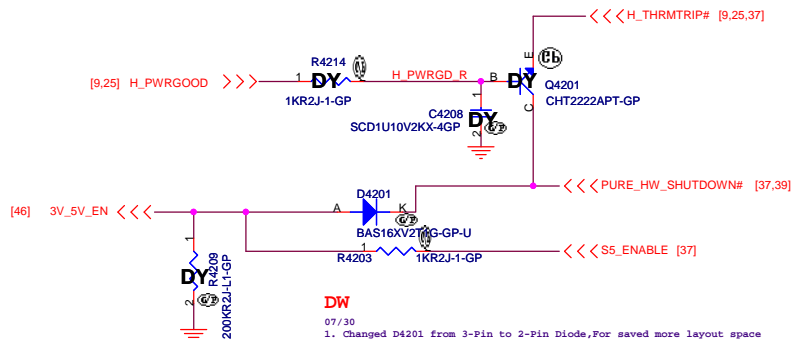
Rev  
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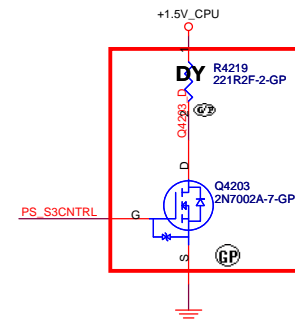
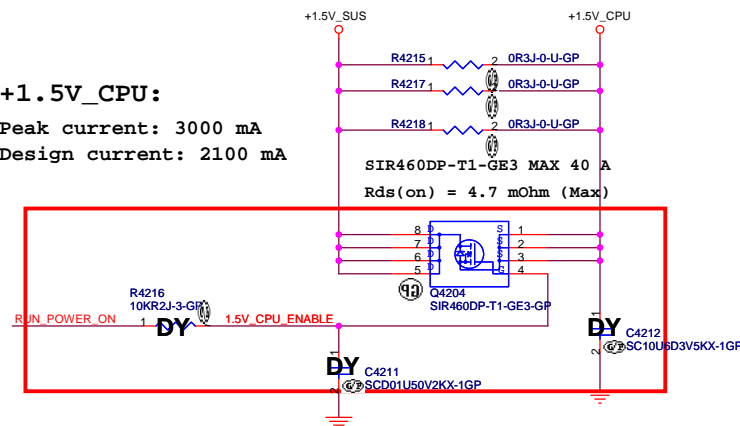
WWW.AliSaler.Com

SSID = Reset.Suspend



### +1.5V\_CPU:

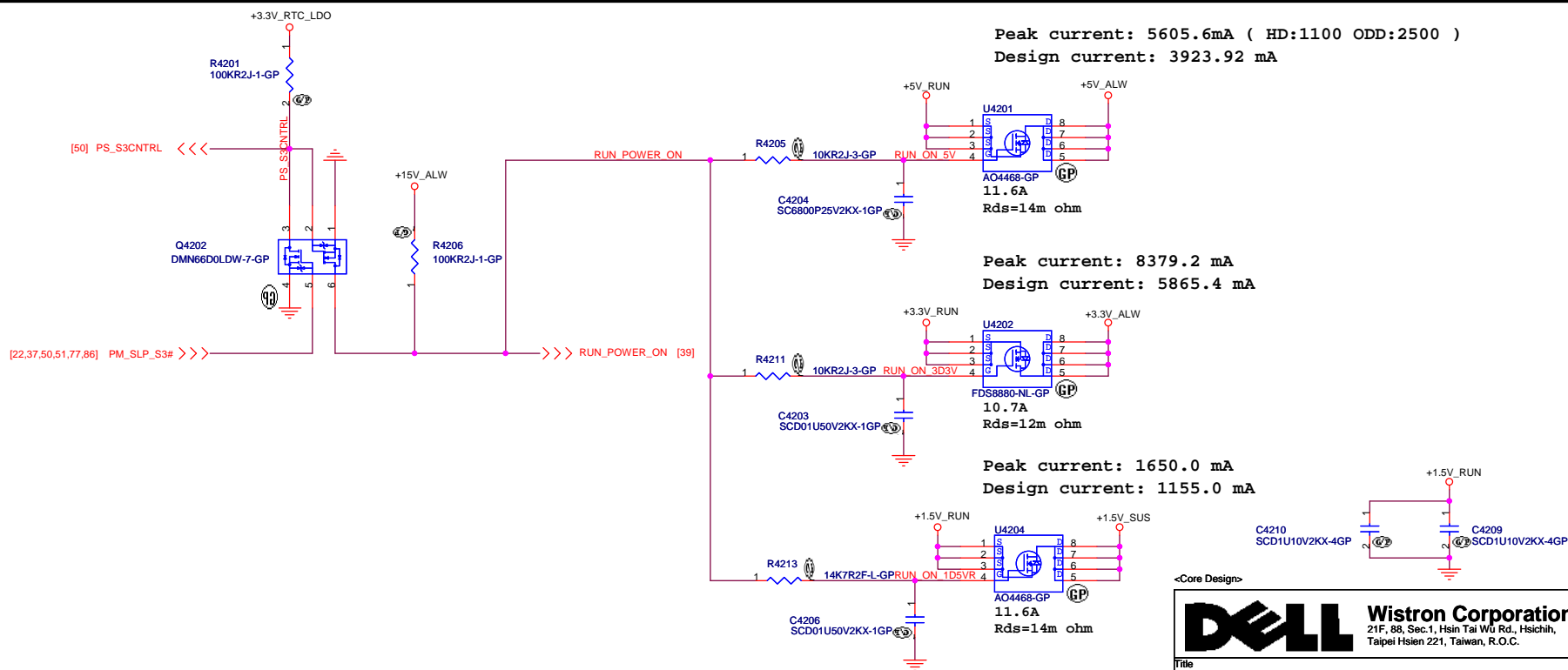
Peak current: 3000 mA  
Design current: 2100 mA



DW  
07/07 Added  
1. Added discharge circuit

Calpella Platform S3 Power Reduction Platform  
S3 Power Reduction CRB Implementation  
Design Details

Revision 0.1

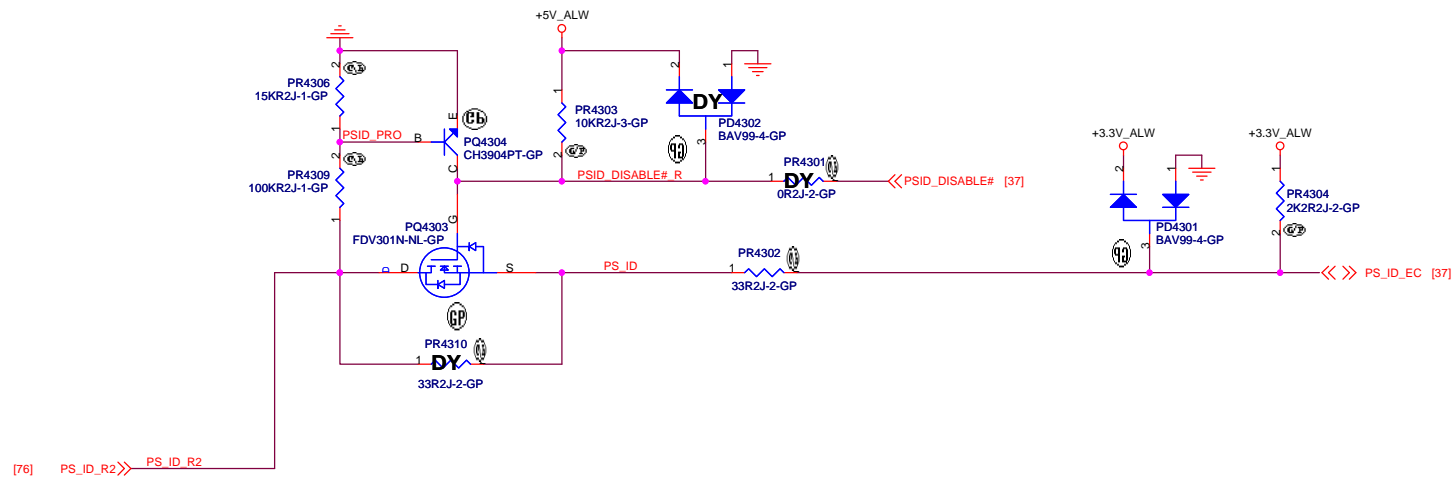


Peak current: 5605.6mA ( HD:1100 ODD:2500 )  
Design current: 3923.92 mA

Peak current: 8379.2 mA  
Design current: 5865.4 mA


Peak current: 1650.0 mA  
Design current: 1155.0 mA

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Title <b>Power Plane Enable</b>		
Size Custom	Document Number <b>Vostro Calpella</b>	Rev <b>SA</b>
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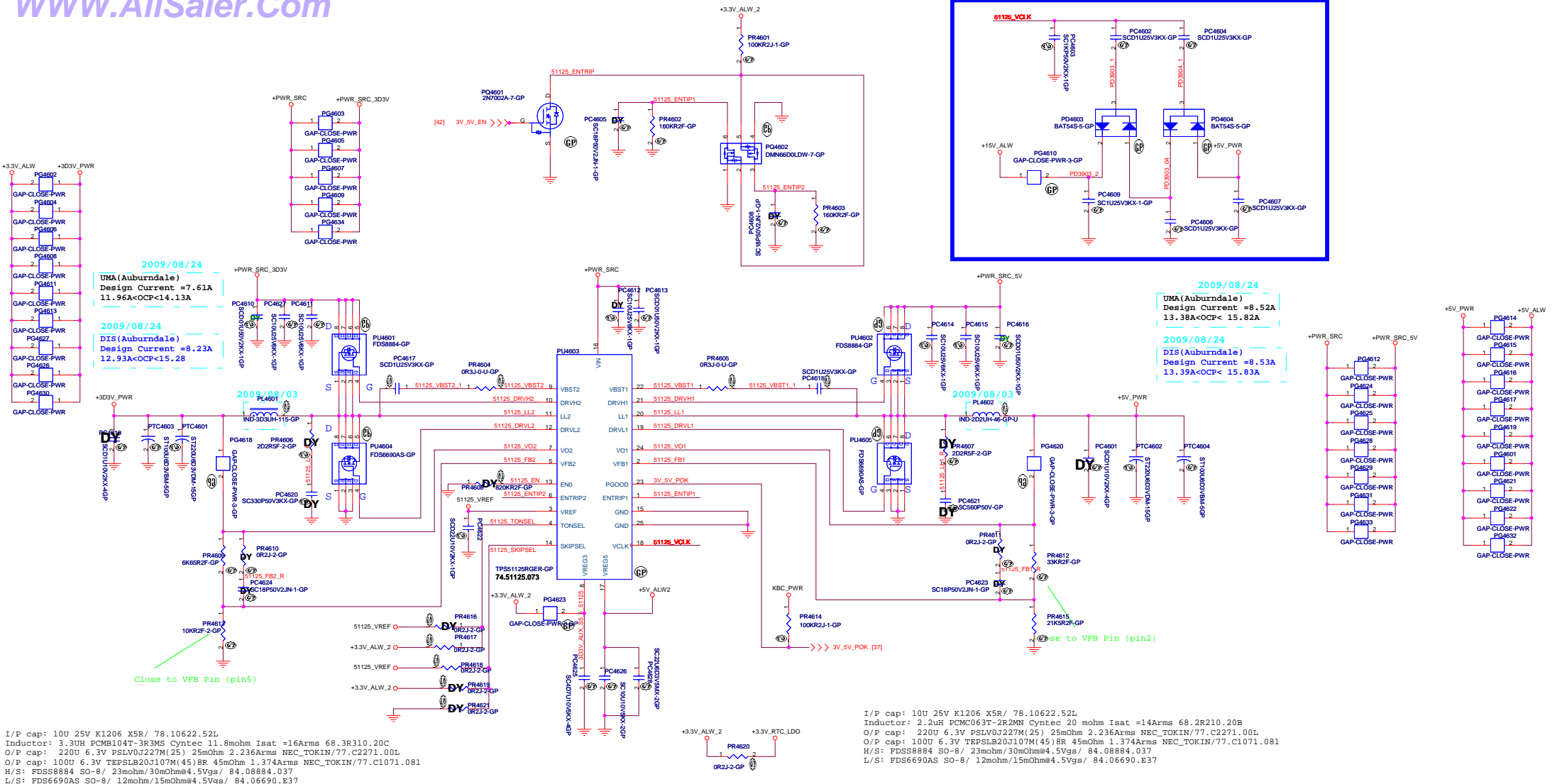
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**Vostro Calpella**

Rev  
**SA**

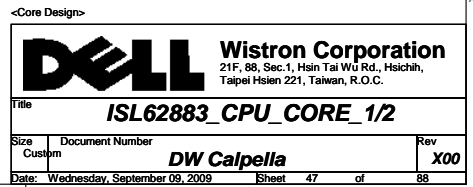
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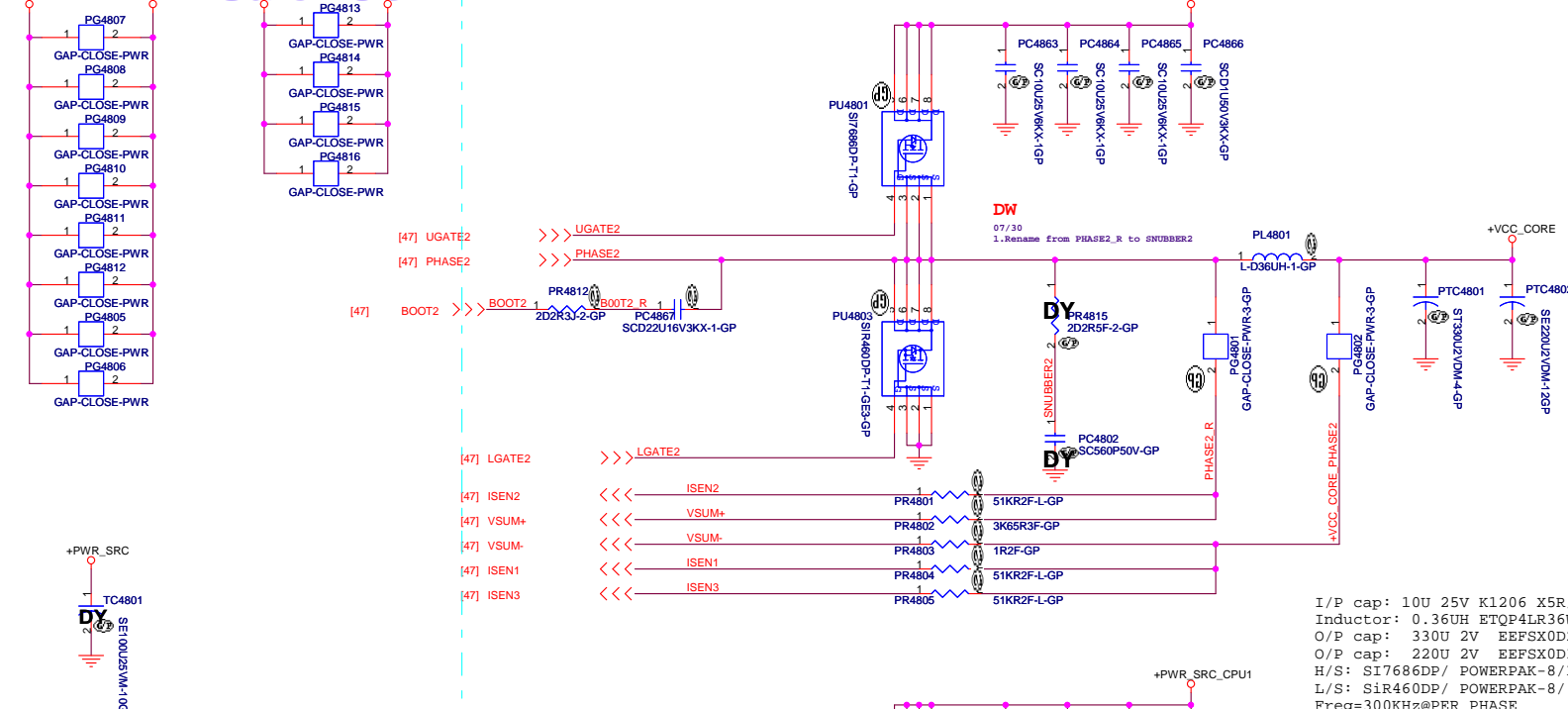


TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

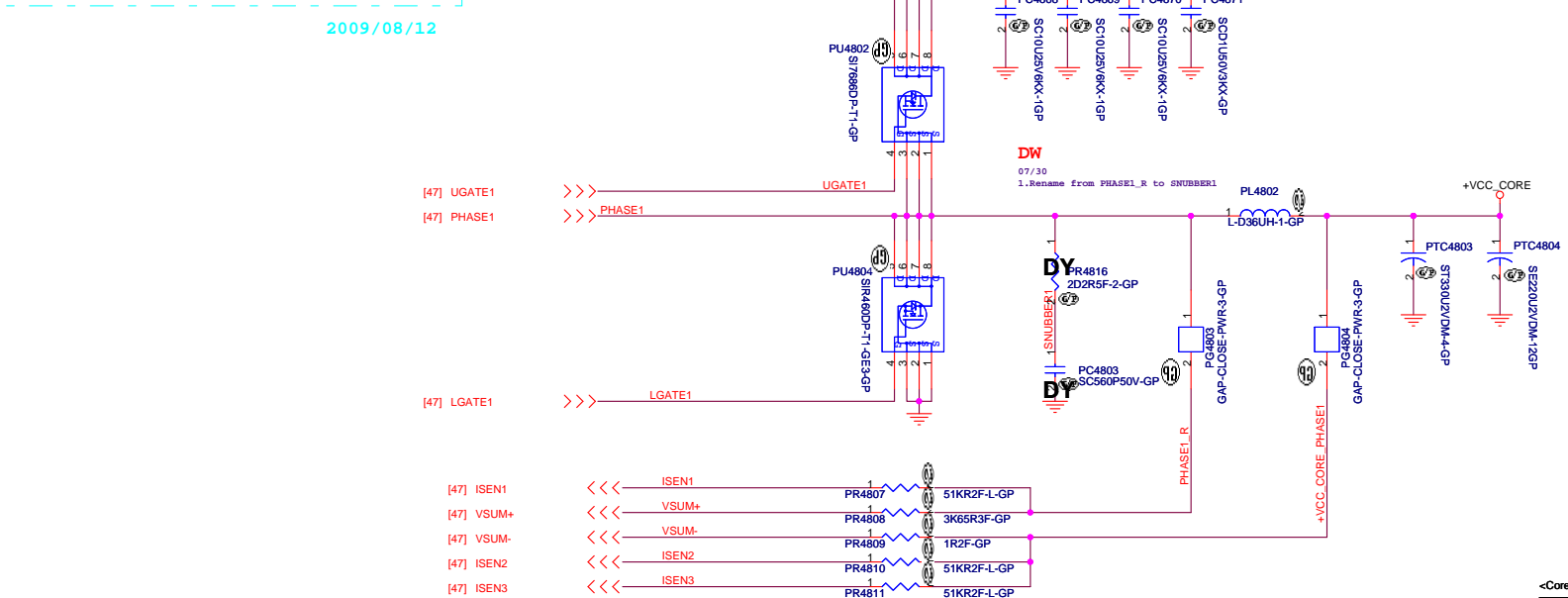




DIS(Auburndale)  
Design Current = 34A  
Peak Current=48A  
57.6A<OCP< 67.2A

UMA(Auburndale)  
Design Current = 34A  
Peak Current=48A  
57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A  
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L  
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037  
Freq=300KHz@PER PHASE

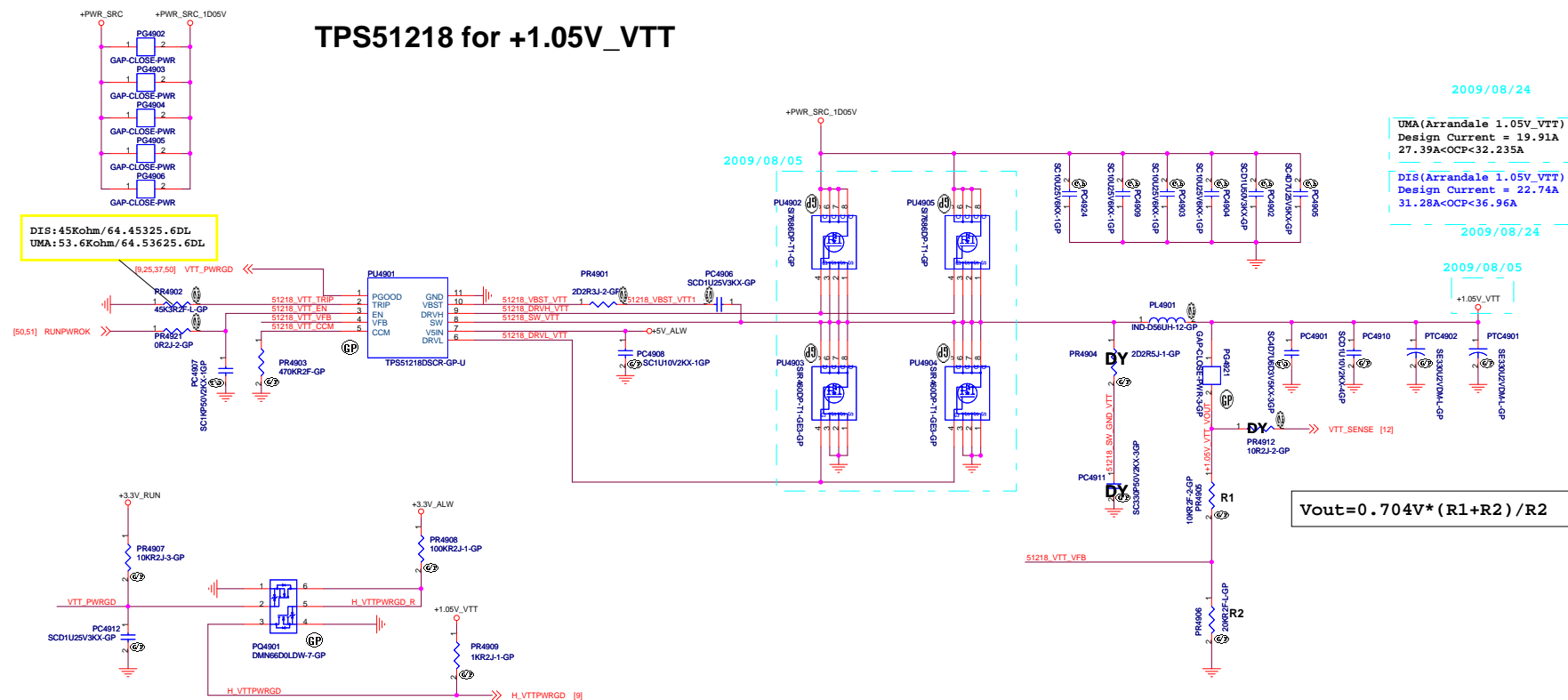


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Title <b>ISL62883_CPU_CORE_2/2</b>					
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## TPS51218 for +1.05V\_VTT



```
Frequency setting
470K  -->290KHz
200K  -->340KHz
100K  -->380KHz
 39K  -->430KHz
```

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56M Cyntec DCR: 1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2.5V EEF5XSD03131ER 90mohm 3Arms PANASONIC/ 79.33719.L01  
H/S: SR474DP-T1-GE3/10mohm/ 12mohm@4.5Vgs/ 84.00474.037  
L/S: SI7170DP-T1-GE3/3.6mohm/ 4.3mohm@4.5Vgs/ 84.07170.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

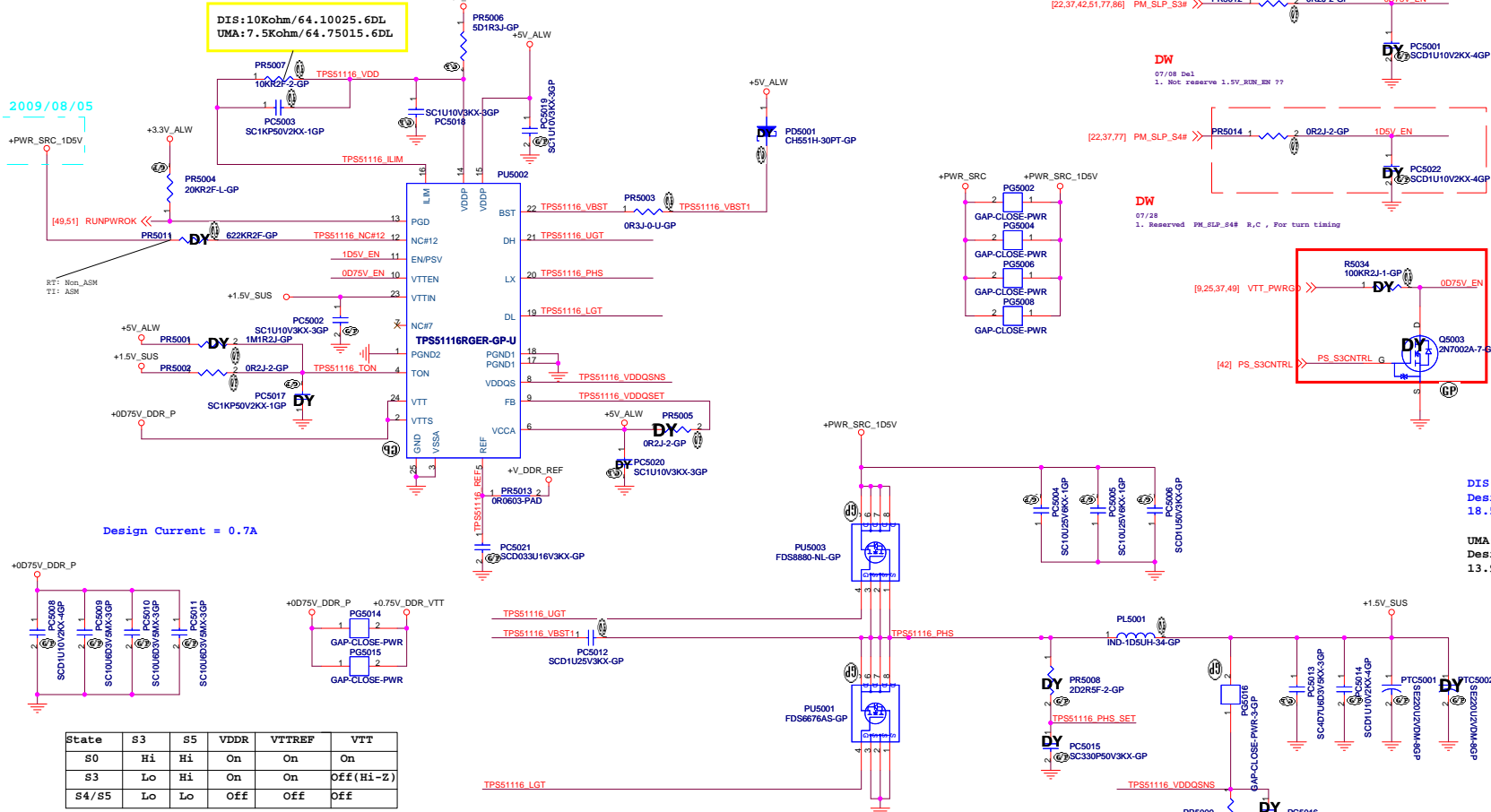
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Title			
<b>TPS51218 +1.05V VTT</b>			
Size	Document Number		Rev
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SSID = PWR.Plane.Regulator\_1p5v0p75v

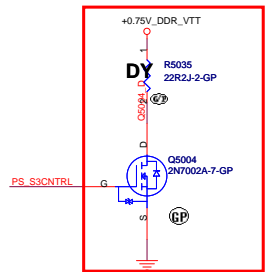
2009/08/05



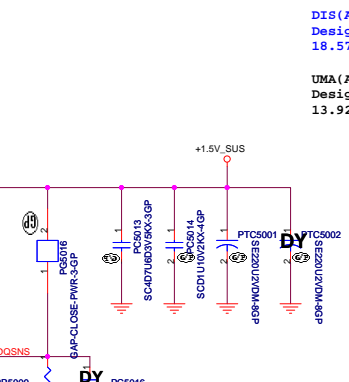
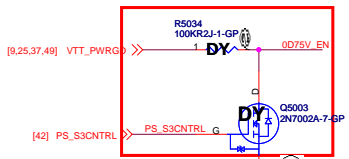
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VDDQSNS/2	DDR
V5IN	1.8	VDDQSNS/2	DDR2
FB Resistors	Adjustable	VDDQSNS/2	1.5 V < VDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 220U 2V EBFCK0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L  
H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037  
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37  
Switching freq-->400KHz

DIS(Auburndale)  
Design Current = 11.82A  
18.57A<OCP<21.95A  
UMA(Auburndale)  
Design Current = 8.86A  
13.92A<OCP<16.45A



425302\_425302\_Calpella\_S3PowerReduction\_WhitePape  
Revision 0.7



Close to VFB Pin (pin5)

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 +1.5V\_SUS**

Size: Custom	Document Number: <b>425302</b>	Rev: <b>X00</b>
Date: Wednesday, September 09, 2009		Sheet: 50 of 88

## APL5930 for +1.8V\_RUN

[illegible]

**<Core Design>**

( Blank )

<Core Design>

DELL

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
Custom

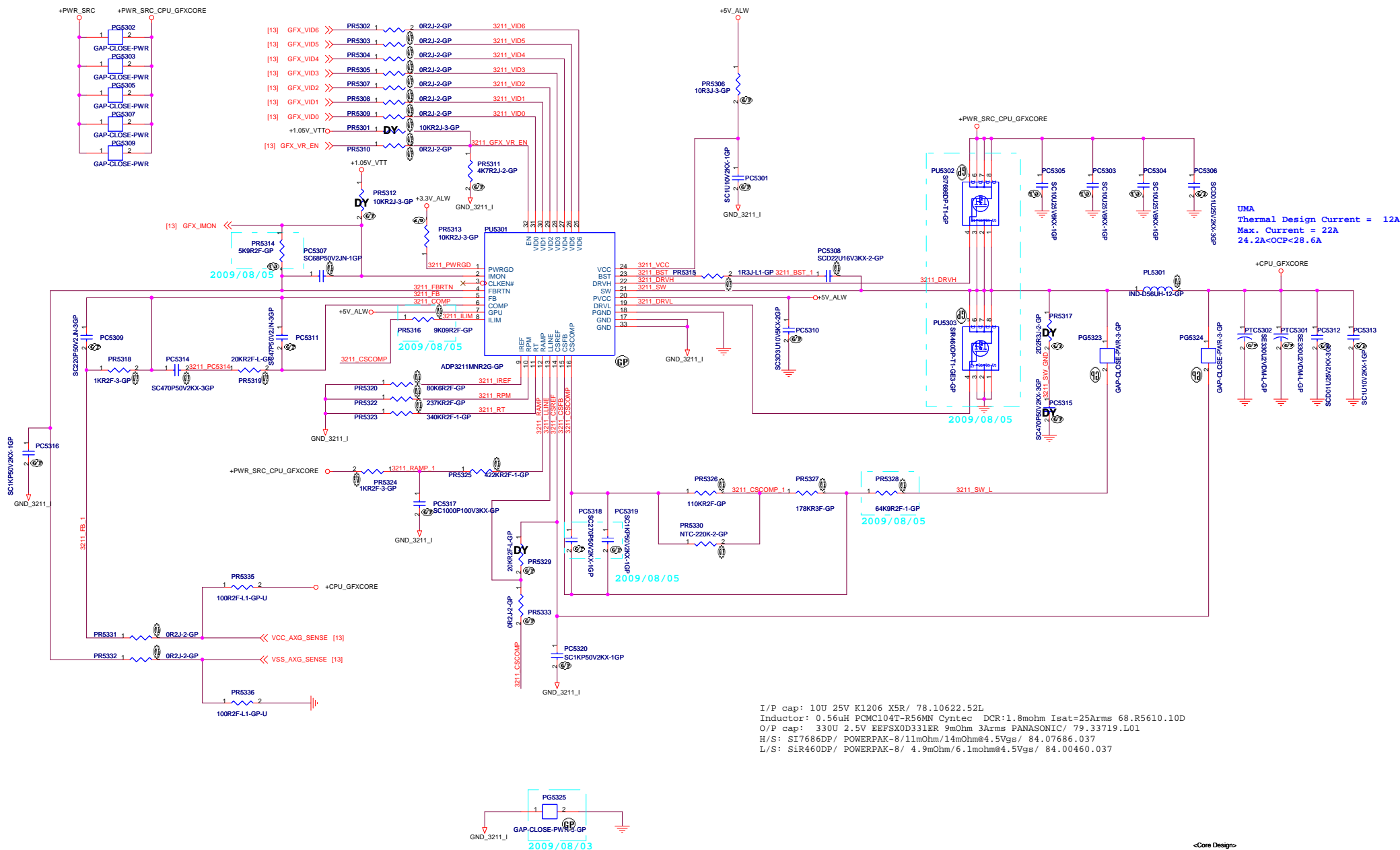
Document Number  
**Vostro Calpella**

Rev  
**SA**

Date: Wednesday, September 09, 2009Sheet 52 of 88

(Reserve)

```
SSID = CPU.GFX.Regulator
```



I/P cap: 10U 25V KI206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56M Cymtec DCR:1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2.5V EEFSX043131ER ERM 3Arms PANASONIC/ 79.33719.L01  
H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SIR4640DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.03D

### <Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>ADP3211 CPU GFXCORE</b>			
Size	Document Number	Rev	
Custom	<b>DW Calpella UMA</b>	<b>X00</b>	
Date: Wednesday, September 09, 2009		Sheet 53	of 88

SSID = VIDEO

Close PCH

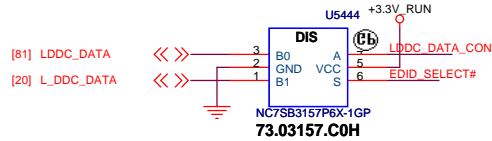
Close GPU

DW

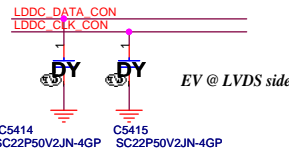
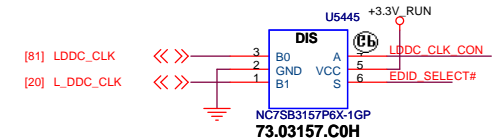
07/07 Added  
1. Added LVDS DDC CLK/DAT Pull Hi

### UMA/DIS LVDS DDC CLK/DAT select circuit

H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)



[23,55,57] EDID\_SELECT# >>> EDID\_SELECT#



EV @ LVDS side

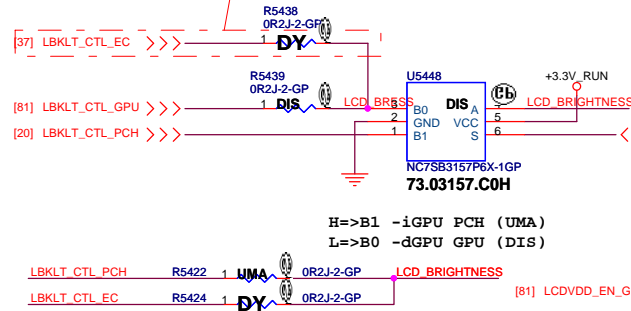
2009/05/25

DW

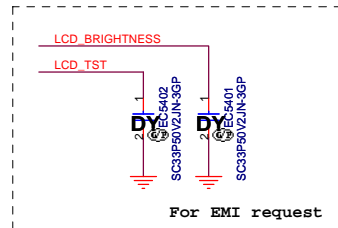
07/05  
1. LCD brightness control are separated by GPU,PCH,EC  
2. LCD Power Enable control are separated by GPU,PCH,EC  
07/23  
1. Added LCD brightness control by EC  
07/28  
1. Removed LCD brightness control with EC and GPU

### UMA/DIS LVDS PWM select circuit

H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)



2009/06/19



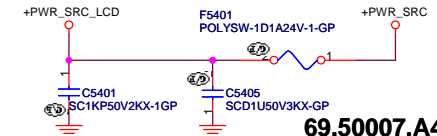
For EMI request

DW

07/30  
1. Changed D5407 from 3-Pin to 2-Pin Diode, For saved more layout space

SSID = Inverter

### INVERTER POWER



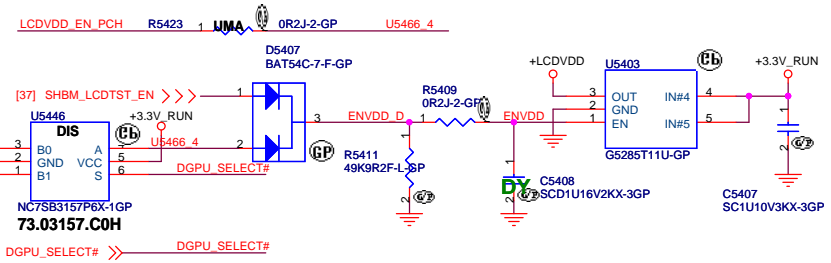
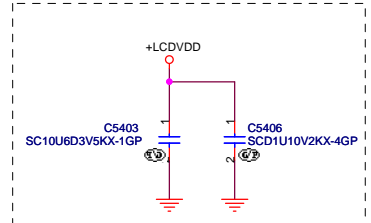
2ND : 69.50007.A31

DW

08/18  
1. Changed F5401 P/N from 69.43001.101 to 69.50007.A41,  
For new projects need changed panel PWRSRC use poly-fuse instead of fuse.

SSID = VIDEO

### LCD POWER



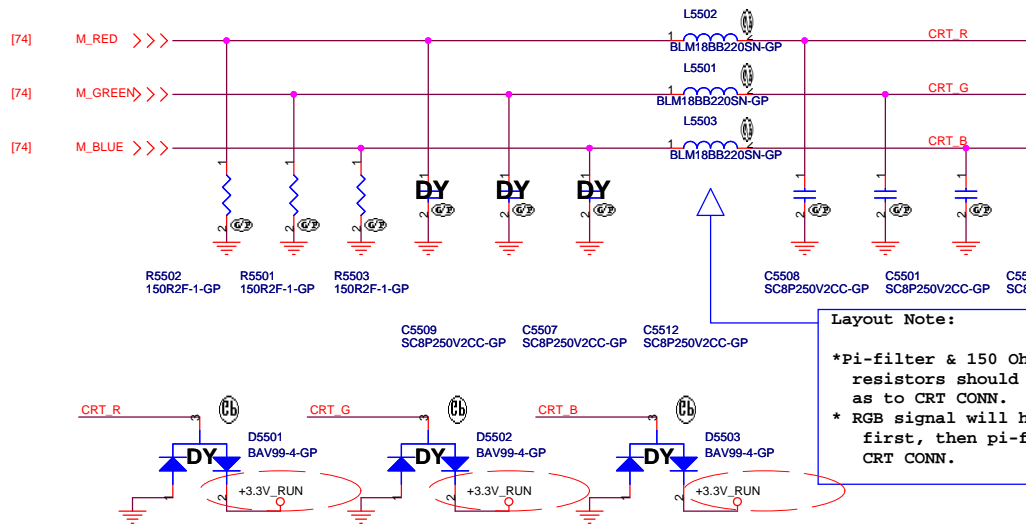
H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)

<Core Design>

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

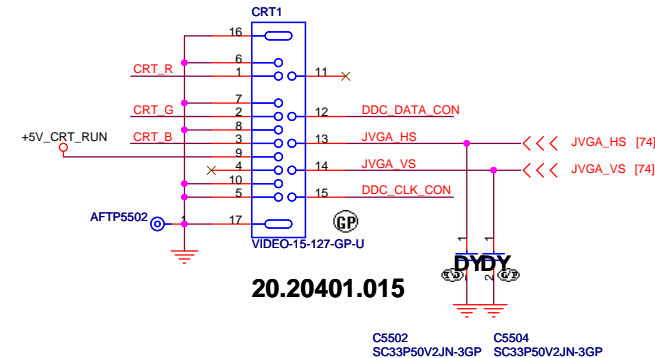
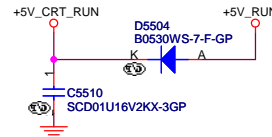
Title			Rev
LCD/Inverter Connector			SA
Size	Document Number		
Custom	Vostro Calpella		
Date	Wednesday, September 09, 2009	Sheet	54 of 88

SSID = VIDEO



**Layout Note:**

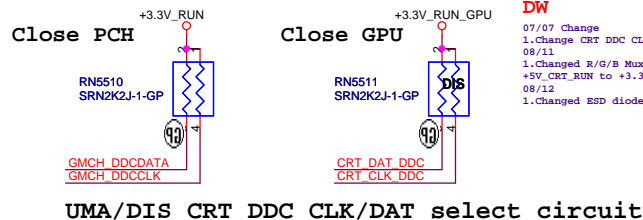
- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



**DW**

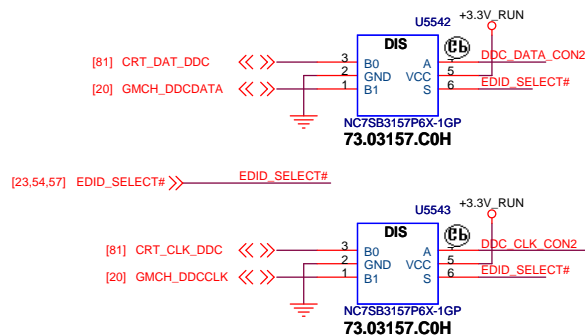
07/14 Change  
1.Change CRT1 CONN PN from 20.20431.015 to 20.20401.015 base on ME emm files.

- AFTP5503 1 +5V\_CRT\_RUN
- AFTP5501 1 DDC DATA CON
- AFTP5509 1 DDC CLK CON
- AFTP5507 1 CRT R
- AFTP5506 1 CRT G
- AFTP5508 1 CRT B
- AFTP5504 1 JVG A HS
- AFTP5505 1 JVG A VS



**DW**

07/07 Change  
1.Change CRT DDC CLK/DAT Circuit  
08/11  
1.Changed R/G/B Mux,ESD diode power rail from +5V\_CRT\_RUN to +3.3V\_RUN\_GPU for correct.  
08/12  
1.Changed ESD diode power rail from +3.3V\_RUN\_GPU to +3.3V\_RUN for power header.



H=>B1 -iGPU PCH (UMA)  
L=>B0 -dGPU GPU (DIS)

GMCH\_DDCDATA R5593 1 UMA 0R2J-2-GP DDC DATA CON2  
GMCH\_DDCCLK R5592 1 UMA 0R2J-2-GP DDC CLK CON2

WWW.AliSaler.Com

<Core Design>

**DELL** Wistron Corporation  
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Title: **CRT Connector**

Size: A3 Document Number: **Vostro Calpella** Rev: SA

Date: Wednesday, September 09, 2009 Sheet: 55 of 88

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<Core Design>

DELL

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size

Custom

Document Number

Vostro Calpella

Rev

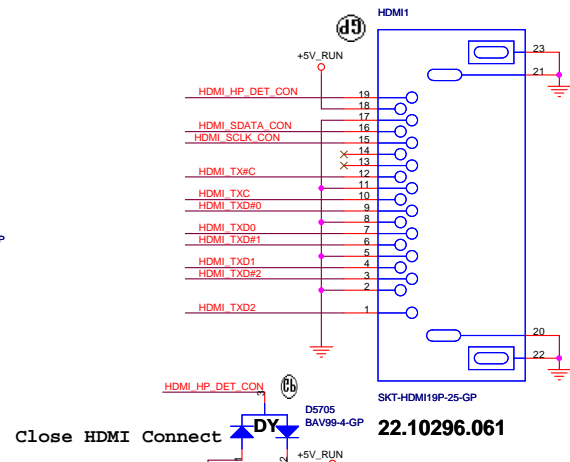
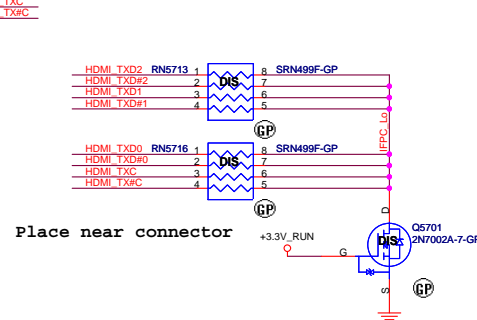
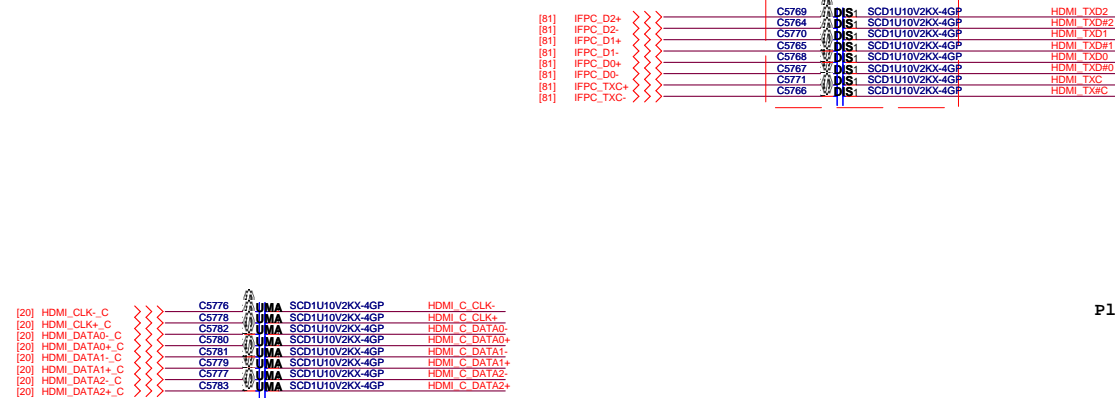
SA

Date: Wednesday, September 09, 2009

Sheet 56 of 88

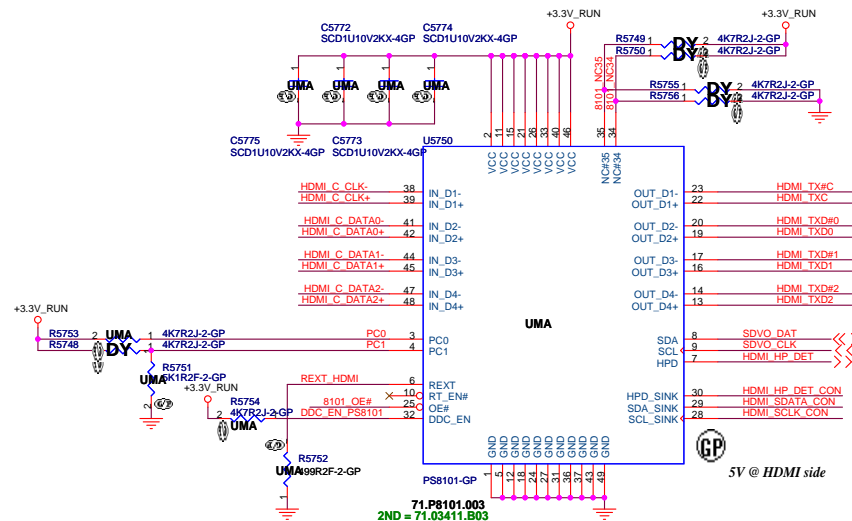


UMA/DIS HDMI signal select circuit  
Place near connector

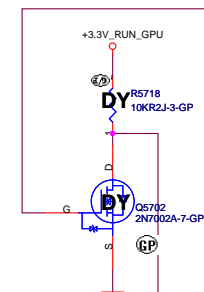
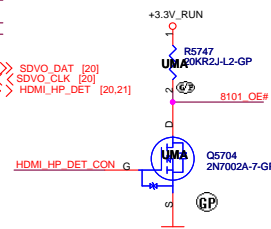
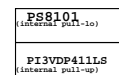


Close to PCH

## UMA HDMI level shift circuit



jitter elimination control

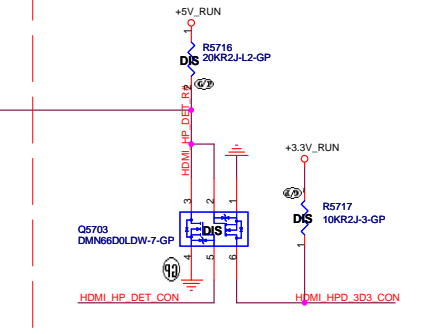


**DW**

07/30 Removed

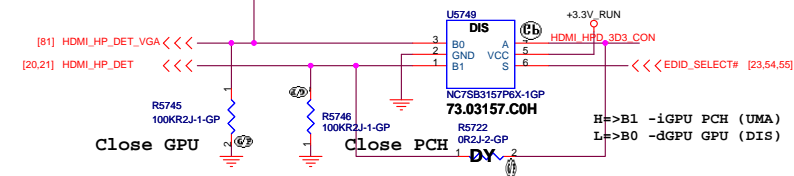
- 1.Removed AFTP Test Point on HDMI,SATA Connector
- 2.Changed HDMI Detection level shift circuit between the Mux and the connector.
- 3.Reserve 0 ohm on HEMI DDC CLK/DAT, between DGPU and ther connector.

## HDMI level shift circuit

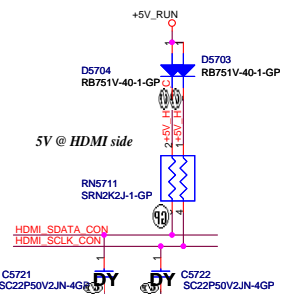
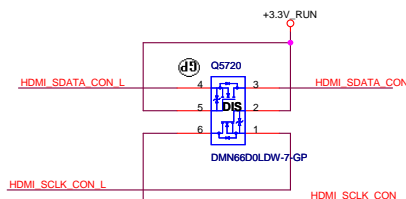
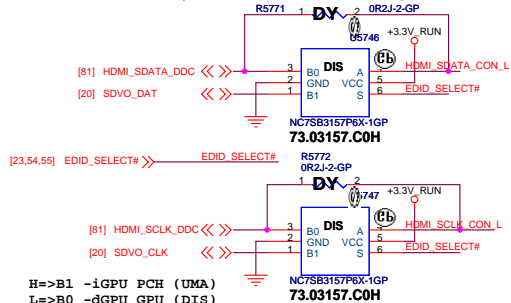


DW  
07/29  
1.HDMI for Un-switched Display , Update Spec.

## UMA/DIS HDMI Detection select circuit



## UMA/DIS HDMI DDC CLK/DAT select circuit



```
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)
```

&lt;Core Design&gt;



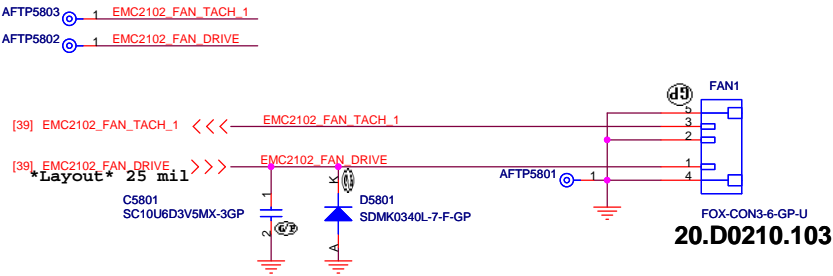
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

### HDMI Connector

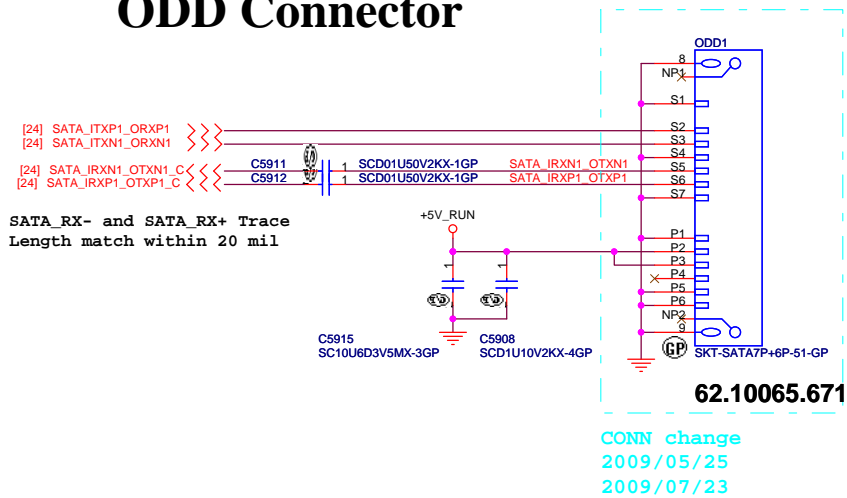
Size	Document Number	Rev
Custom	<b>Vostro Calpella</b>	S

SSID = Thermal

Fan Connector

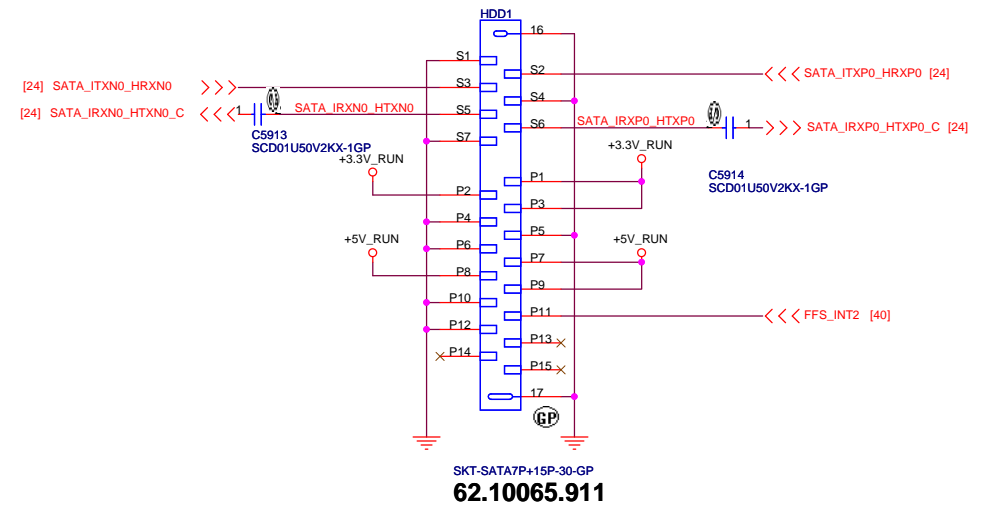


## ODD Connector



DW  
07/30 Removed  
1. Removed AFTP Test Point on HDMI, SATA Connector

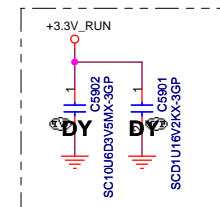
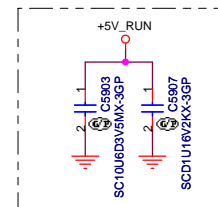
## SATA HDD Connector



Close to CONN  
5V power pin


Close to CONN  
3.3V power pin

DW  
07/30 Removed  
1. Removed AFTP Test Point on HDMI, SATA Connector



(Blank)

<Core Design>



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserve)**

Size	Document Number	Rev
Custom	<b>Vostro Calpella</b>	<b>SA</b>

Date: Wednesday, September 09, 2009	Sheet 60 of 88
-------------------------------------	----------------

(Blank)

<Core Design>

DELL

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size

Custom

Document Number

Vostro Calpella

Rev

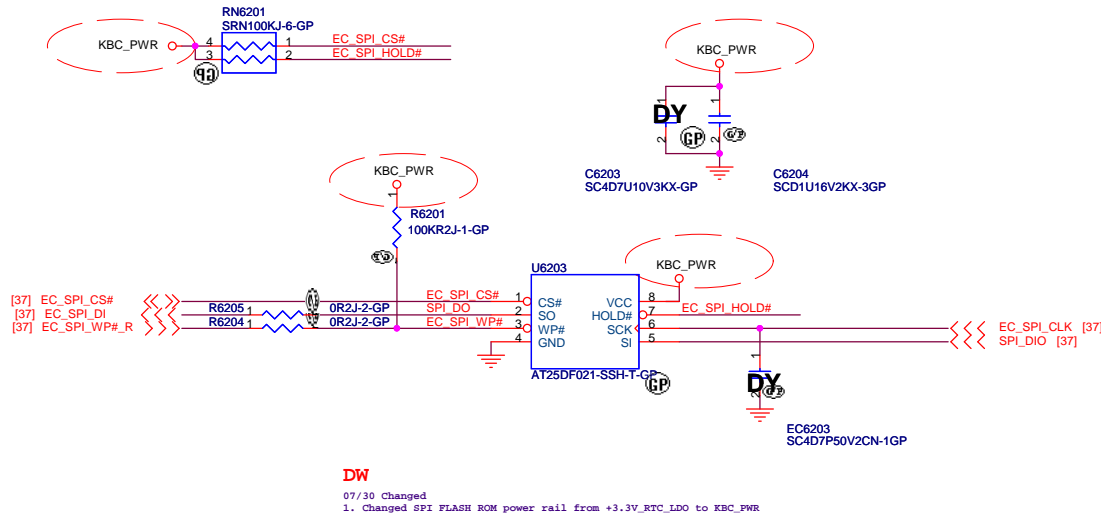
SA

Date: Wednesday, September 09, 2009

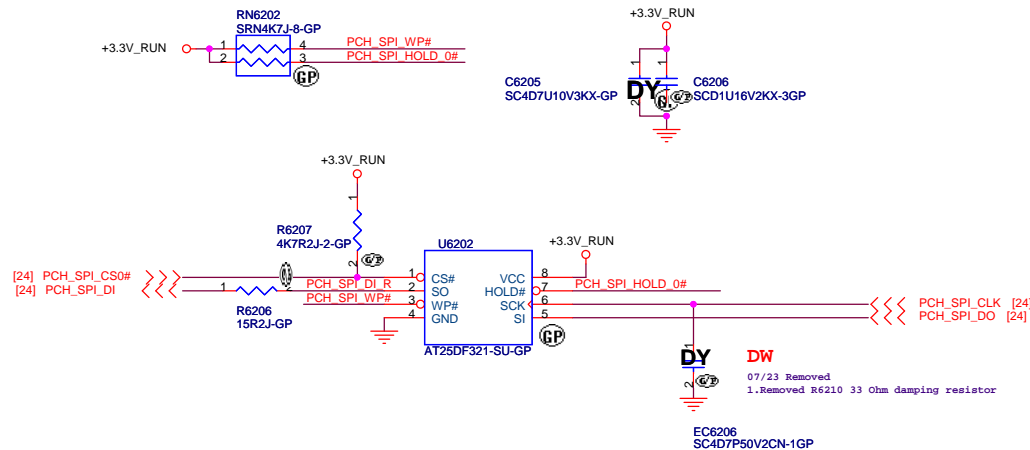
Sheet 61 of 88

SSID = Flash.ROM

## SPI FLASH ROM (256K bytes) for KBC

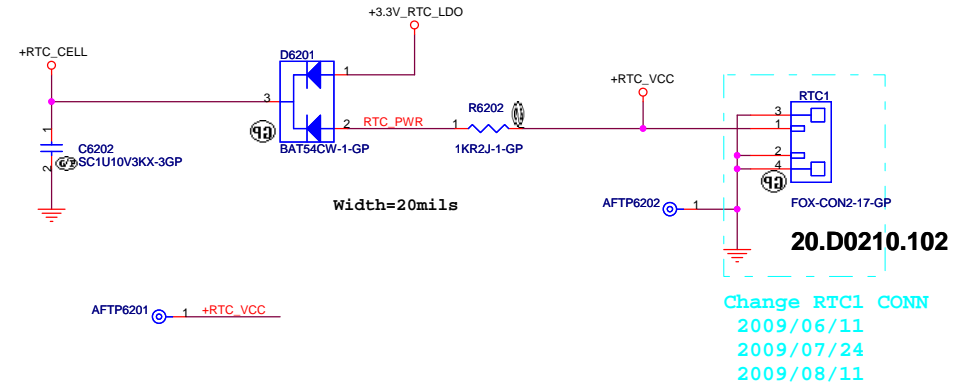


## SPI FLASH ROM (4M bytes) for PCH



SSID = RBATT

## RTC Connector

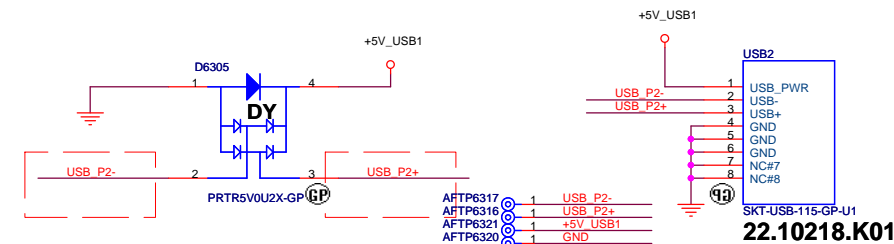
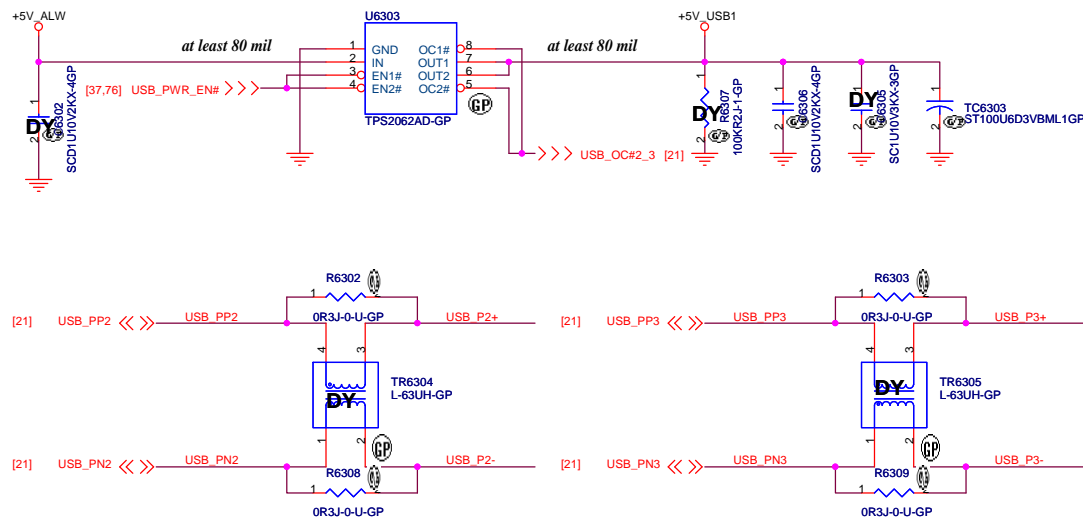


<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

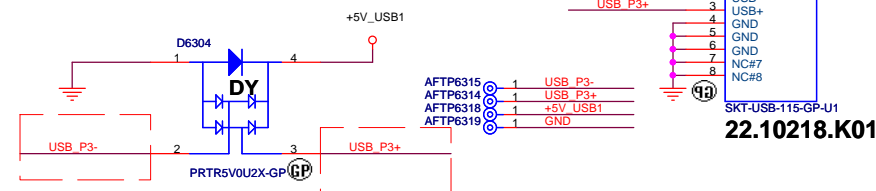
Title		
EEPROM/RTC Connector		
Size	Document Number	Rev
A3	Vostro Calpella	SA
Date:	Wednesday, September 09, 2009	Sheet 62 of 88



DW

07/29

1.Changed USB ESD Protection Diode between the common mode choke and the USB connector data pins



DW

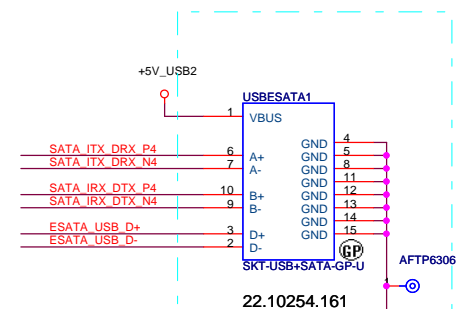
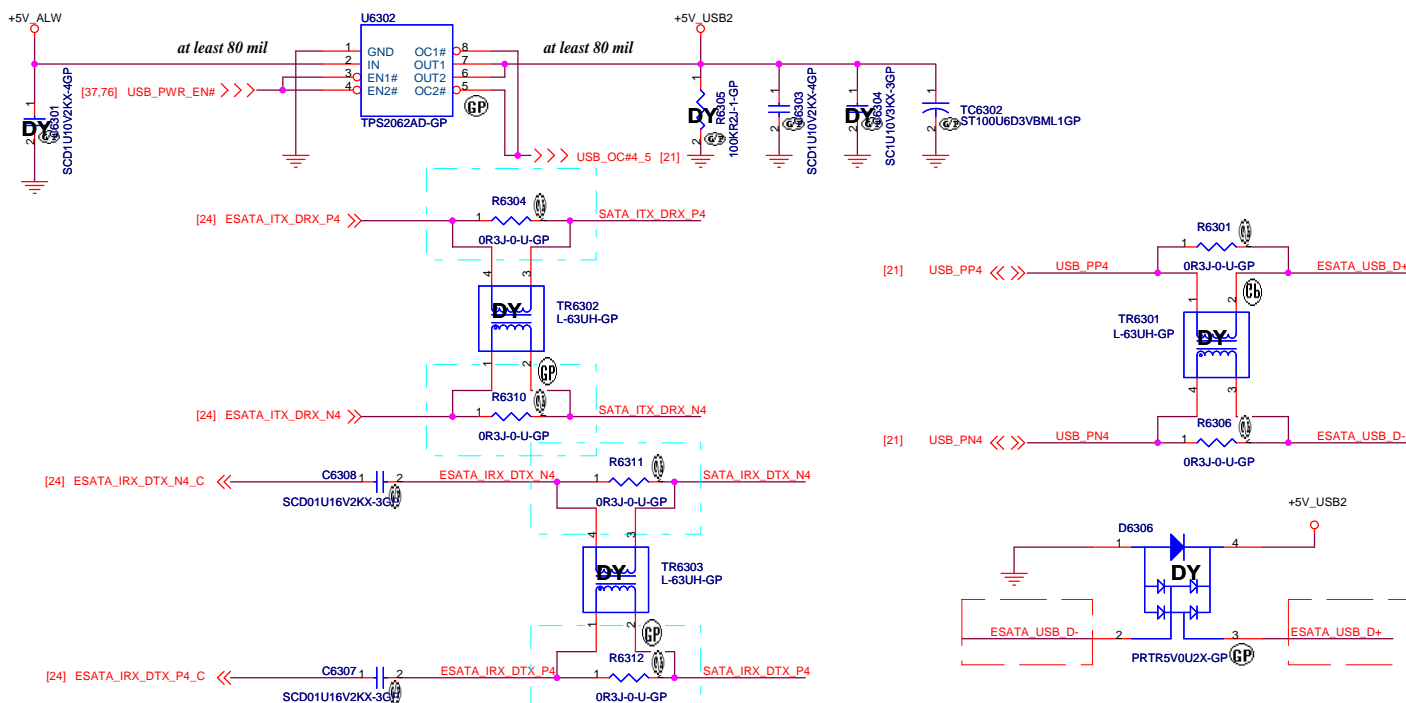
07/14 Change

1.Change USB2,USB3 CONN PN from  
22.10321.001 to 22.10218.T31 base on ME emm files.

Change CONN 2009/05/27

2009/07/23

## ESATA Power

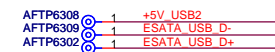


Change CONN 2009/05/27

DW

07/30 Removed

1.Removed AFTP Test Point on HDMI,SATA Connector



## <Core Design>



**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>USB /ESATA Port</b>			
Size	Document Number	Rev	
Custom	<b>Vostro Calpella</b>	<b>SA</b>	
Date:	Wednesday, September 09, 2009	Sheet 63 of	88

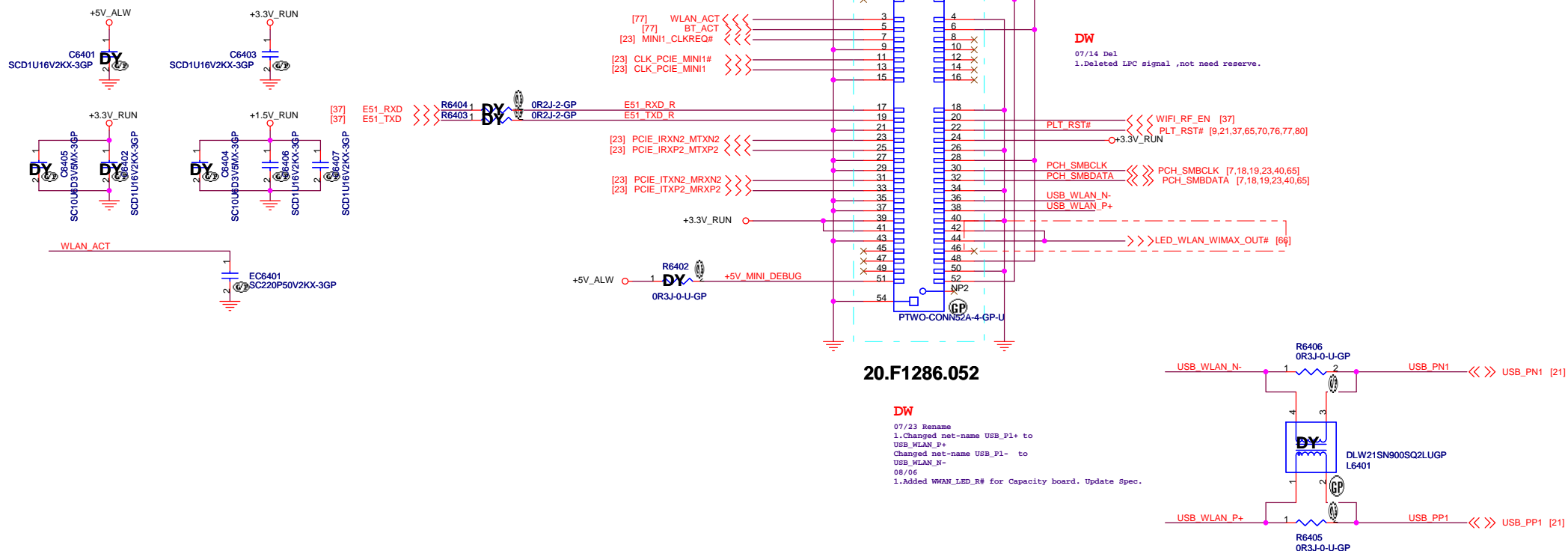
### *Mini Card Connector(802.11a/b/g/n)*

Change CONN

2009/05/25

2009/06/11

2009/07/23



**20.F1286.052**

DW

```
07/23 Rename
1.Changed net-name USB_Pi+ to
USB_WLAN_P+
Changed net-name USB_Pi- to
USB_WLAN_N-
08/06
1.Added WWAN LED R# for Capacity board. Update Spec.
```

## <Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**MINICARD(WLAN)/ITP CONN**

Size

Document Number

## Vostro Calpella

Rev
-----

Date: Wednesday, September 09, 2009

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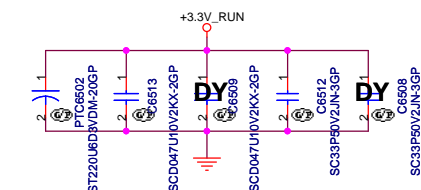
88



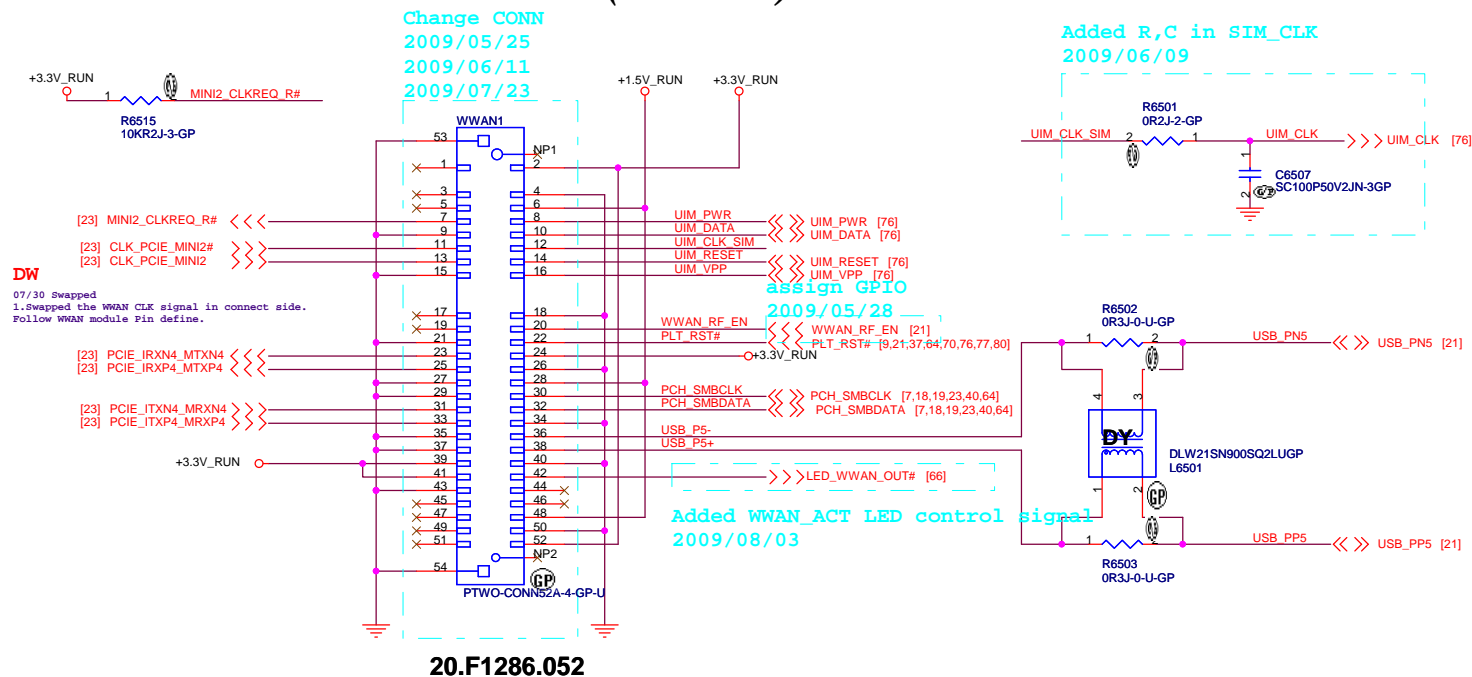
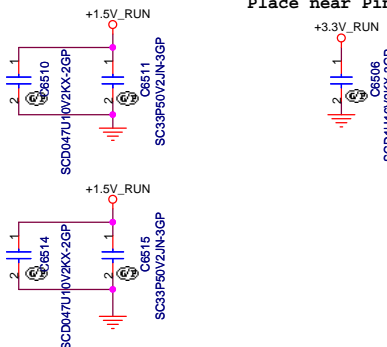
SSID = Wireless

## Mini Card Connector(WWAN)

Place near MINI Card CONN



Place near Pin 24



<Core Design>

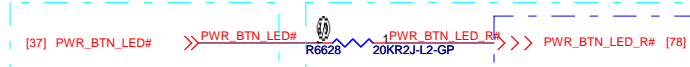
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			WWAN Connector	
Size	Document Number	Rev		
A3	Vostro Calpella	SA		
Date:	Wednesday, September 09, 2009	Sheet	65	of 88

For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WWAN ACT LED	White	RUN
WLAN WIMAX LED	White	RUN

PWR BTN LED



For LED & Capacity board

Added PWR\_BTN\_LED#  
2009/06/04

assign PWR\_BTN\_LED# GPIO

2009/06/09

SCRLK LED



For LED & Capacity board:

CAPS LED



NUM LED



Remove BJT to daughetr board  
2009 06/01

assign GPIO  
2009/05/28

Bluetooth LED

For LED & Capacity board:

DW

08/12

1. Changed WWAN LED & WLAN WIMAX\_LED . for Capacity board. Update Spec.



For IO board

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

WWAN LED



For LED&Capacity board:

WLAN WIMAX\_LED



For LED&Capacity board:

DW

07/28

1. Update R6625 from 10k to 20k ohm

08/05

1.Added WWAN\_LED\_R#,WLAN\_LED\_R# for Capacity board. Update Spec.

08/11

2.Removed BAT1\_LED from Capacity board. Update Spec.

DW

07/28

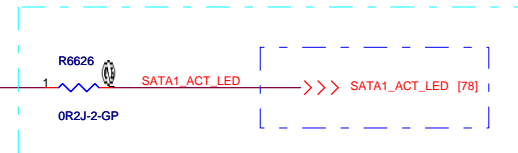
1. Change Power & Battery LED from common-cathode to common-anode

, Modified LED circuitry

08/11

1.Changed battery LED be one LED with bi-color (white and amber). for Capacity board. Update Spec.

HD LED

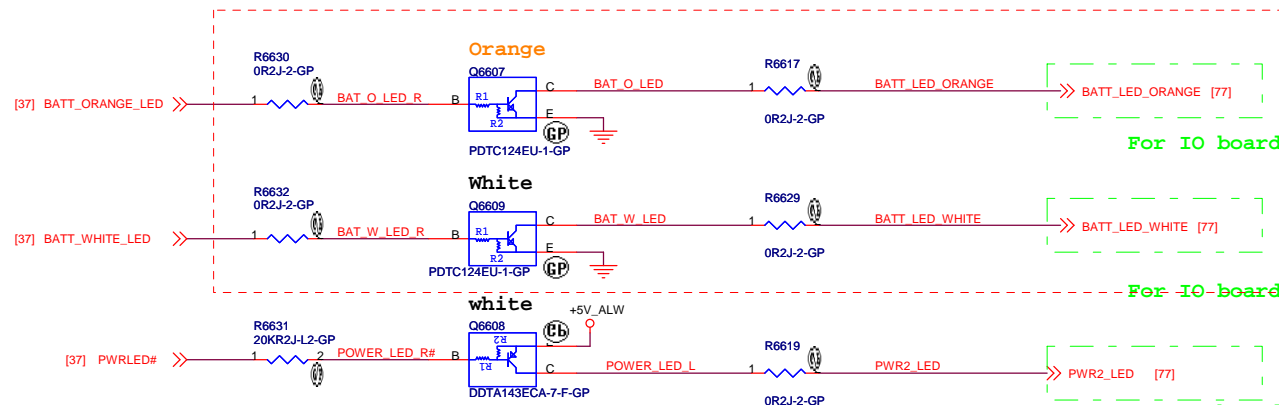


DW

07/29

1. Removed SATA2\_ACT\_LED from I/O board connector.

Battery & Power LED



For IO board

For IO-board

For IO board


<Core Design>

**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LED	
Size A3	Document Number	Rev SA
Date: Wednesday, September 09, 2009	Vostro Calpella	
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<Core Design>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

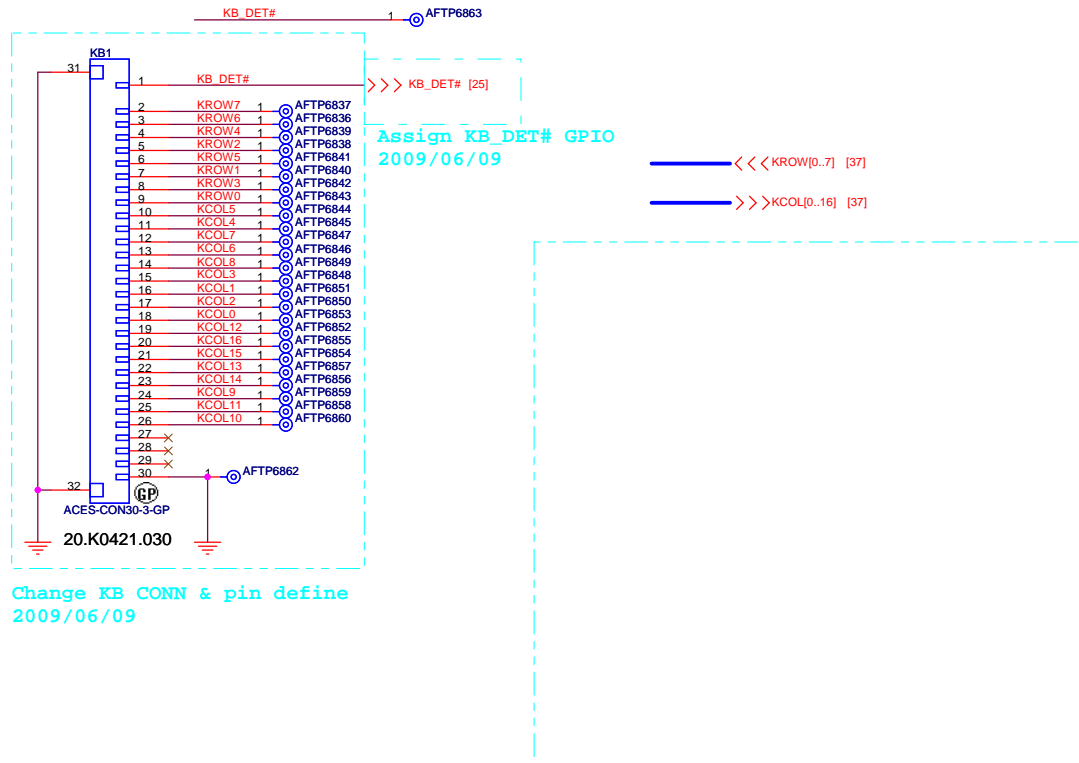
**(Reserve)**

Size	Document Number	Rev
Custom	<b>Vostro Calpella</b>	<b>SA</b>

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SSID = KBC

### Internal Keyboard Connector

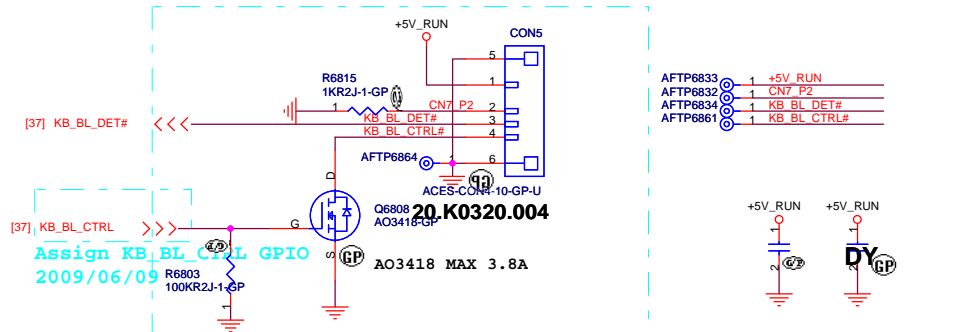


Change KB CONN & pin define  
2009/06/09

Added KB1 EMI Cap  
2009/06/17

DW  
07/27 Removed  
1.Removed KB1 EMI Cap

### KB Backlight CONN

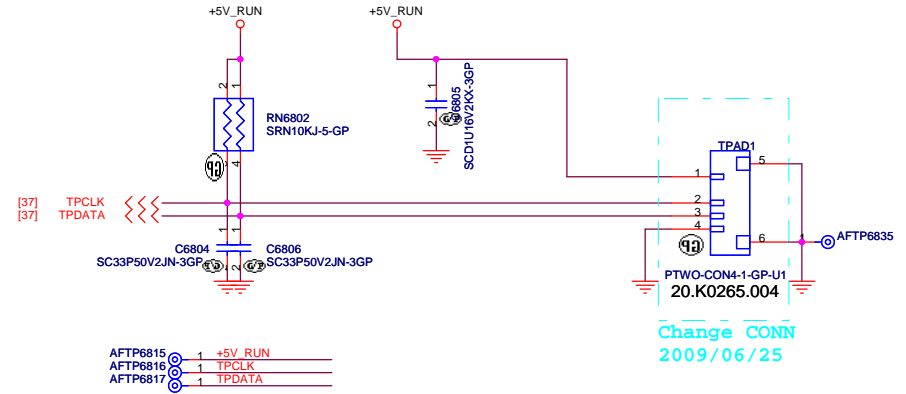


Added KB Backlight CONN  
2009/06/08

Modified CONN7 pin define & added N-MOS  
2009/06/09

SSID = Touch.Pad

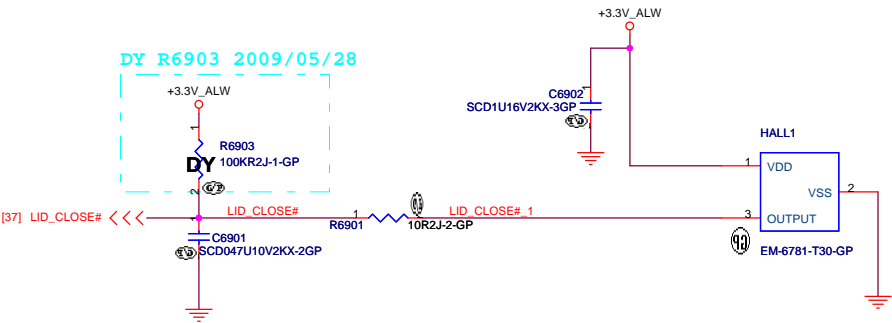
### TouchPad Connector

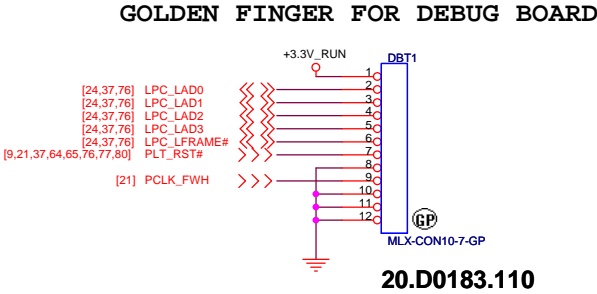


<Core Design>

<b>DELL</b> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Keyboard/Touch Pad</b>		
Size Custom	Document Number <b>Vostro Calpella</b>	Rev <b>SA</b>
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Hall Sensor Connector





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<Core Design>

DELL

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
Custom

Document Number  
**Vostro Calpella**


Rev  
**SA**

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(Reserve)

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	<b>Vostro Calpella</b>	<b>SA</b>

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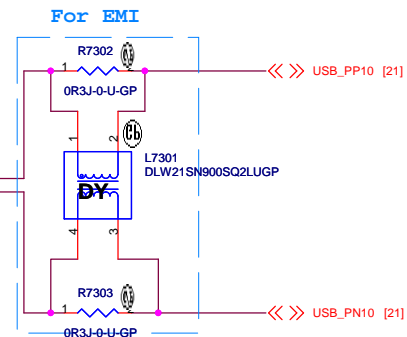
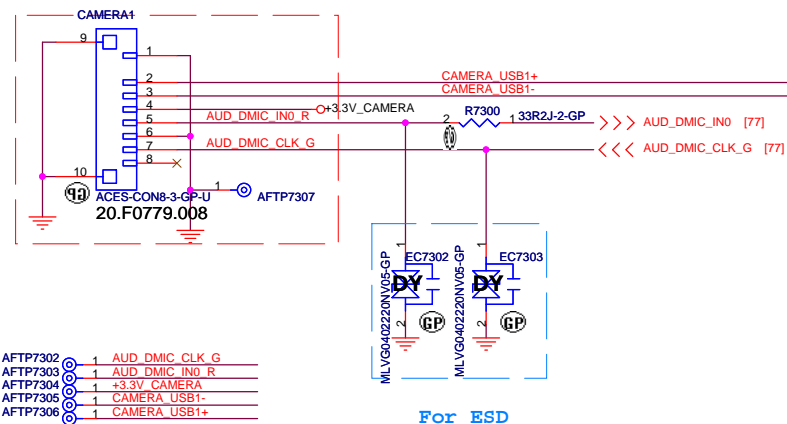
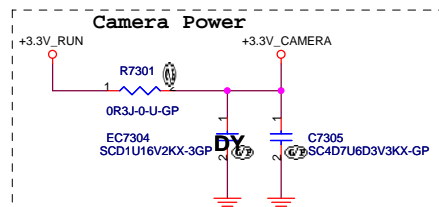


SSID = User.Interface

DW

07/23 Reversal  
 1.CAMERA1 signal Reversal  
 ( 8 -> Detect , 7 -> Gnd , ...1 -> Gnd , 2 -> USB\_D+ )  
 07/27  
 1.Reversal Pin 6 <-> 7 , For Cable Pin define

## Camera Connector



&lt;Core Design&gt;



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Title

Camera CONN

Size

Document Number

Rev

A3

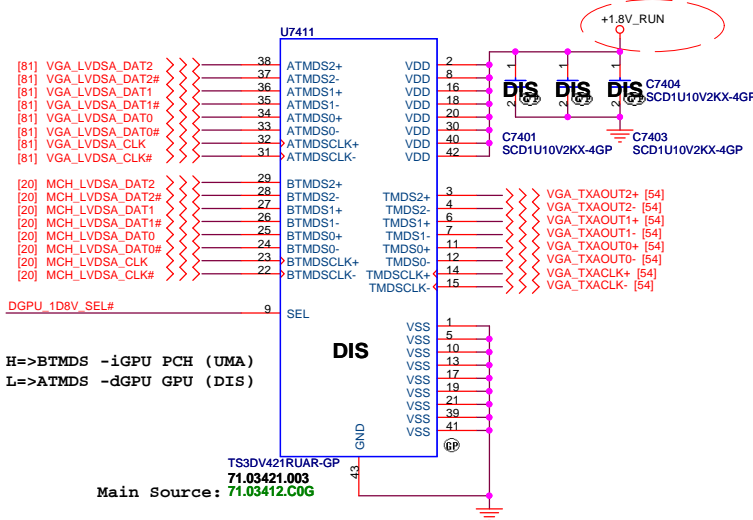
Vostro Montevina Discrete

SA

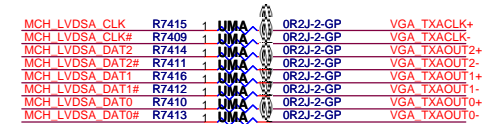
Date: Wednesday, September 09, 2009

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# UMA/DIS LVDS signal select circuit



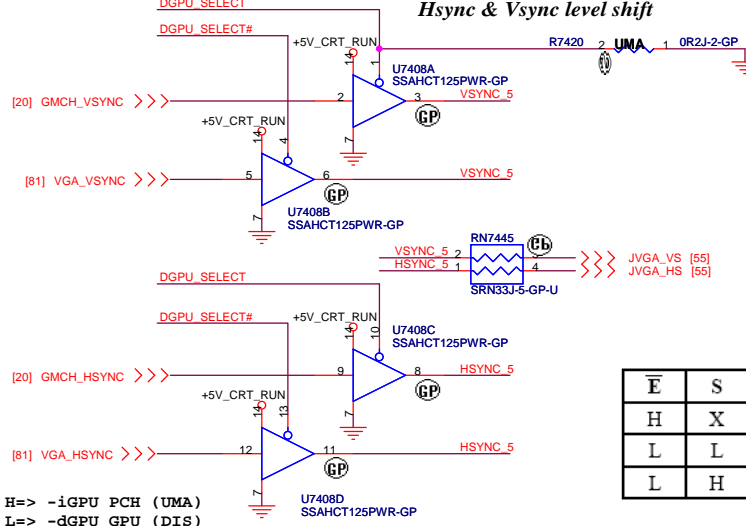
## UMA LVDS signal circuit



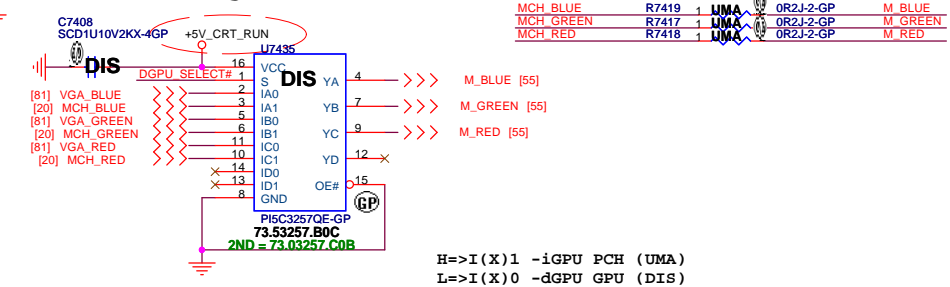
### FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

## UMA/DIS CRT Hsync/Vsync select circuit



## UMA/DIS CRT signal select circuit




$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Swith-1			
Size	Document Number	Rev	
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Vostro Calpella**

Rev  
**SA**

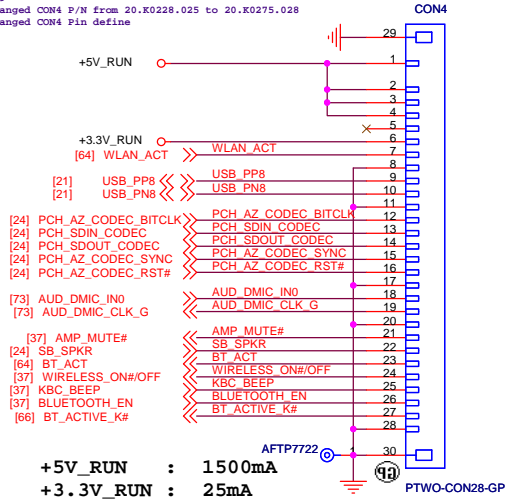
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DW

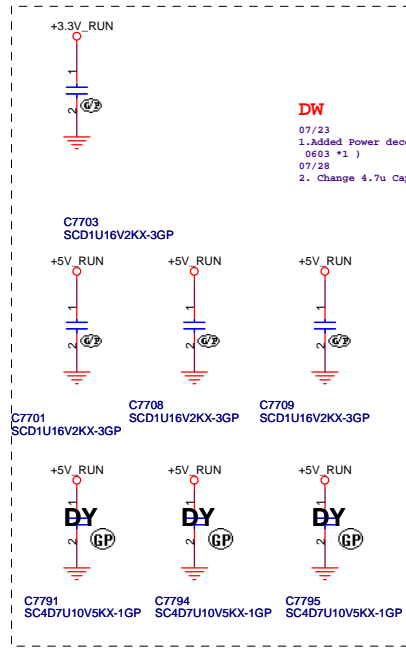
07/08 Not reserve  
1. Not reserve BLUETOOTH\_DET ??  
07/15 Change Power rail  
1. Changed CON4.4 per rail from +1.5V\_RUN to +15V\_ALW  
07/23  
1. Removed +15V\_ALW  
07/29  
1. Changed CON4 P/N from 20.K0228.025 to 20.K0275.028  
1. Changed CON4 Pin define

## Audio board CON



20.K0275.028

Place near CON4

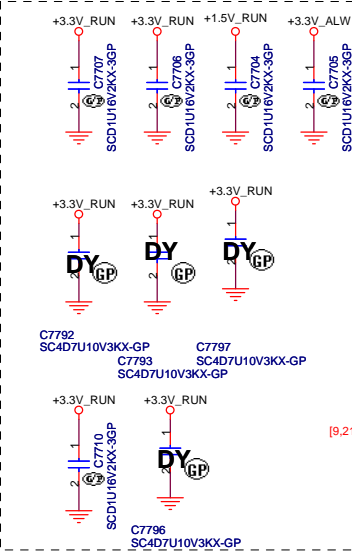


AFTP7710	1	+5V_RUN
AFTP7706	1	+3.3V_RUN
AFTP7709	1	WIRELESS_ON#/OFF
AFTP7702	1	WLAN_ACT
AFTP7703	1	BLUETOOTH_EN
AFTP7704	1	BT_ACTIVE_K#
AFTP7705	1	BT_ACT
AFTP7707	1	USB_PP8
AFTP7708	1	USB_PN8
AFTP7712	1	PCH_AZ_CODEC_BITCLK
AFTP7713	1	PCH_SDIN_CODEC
AFTP7714	1	PCH_SDOUT_CODEC
AFTP7715	1	PCH_AZ_CODEC_SYNC
AFTP7716	1	PCH_AZ_CODEC_RST#
AFTP7718	1	SB_SPKR
AFTP7719	1	KBC_BEEP
AFTP7720	1	AUD_DMIC_IN0
AFTP7721	1	AUD_DMIC_CLK_G
AFTP7723	1	AMP_MUTE#

DW

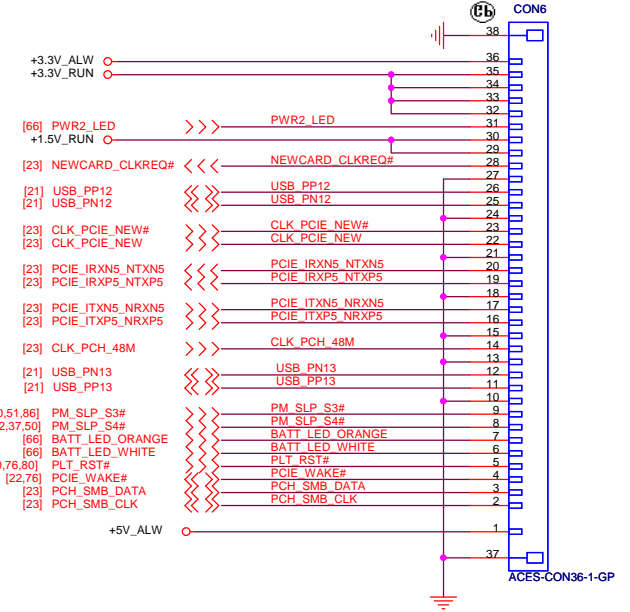
07/23  
1. Added Power decoupling capacitor pre-0.5A ( 0402\*1 0603 \*1 )  
07/28  
2. Change 4.7u Capacitor from 0603 to 0805, for cost

Place near CON6



AFTP7758	1	+3.3V_ALW
AFTP7757	1	+3.3V_RUN
AFTP7760	1	+1.5V_RUN
AFTP7762	1	USB_PN12
AFTP7759	1	USB_PP12
AFTP7769	1	NEWCARD_CLKREQ#
AFTP7768	1	PCH_SMB_CLK
AFTP7767	1	PCH_SMB_DATA
AFTP7771	1	PM_SLP_S3#
AFTP7772	1	BATT_LED_ORANGE
AFTP7781	1	PLT_RST#
AFTP7785	1	BATT_LED_WHITE
AFTP7787	1	+5V_ALW
AFTP7771	1	CLK_PCIE_NEW#
AFTP7770	1	CLK_PCIE_NEW
AFTP7761	1	PCIE_IRXN5_NTXN5
AFTP7765	1	PCIE_IRXP5_NTXP5
AFTP7764	1	PCIE_ITXN5_NRXN5
AFTP7763	1	PCIE_ITXP5_NRXP5
AFTP7775	1	USB_PN13
AFTP7766	1	USB_PP13
AFTP7774	1	PCIE_WAKE#
AFTP7778	1	CLK_PCH_48M

## IO board CON



20.K0276.036

DW

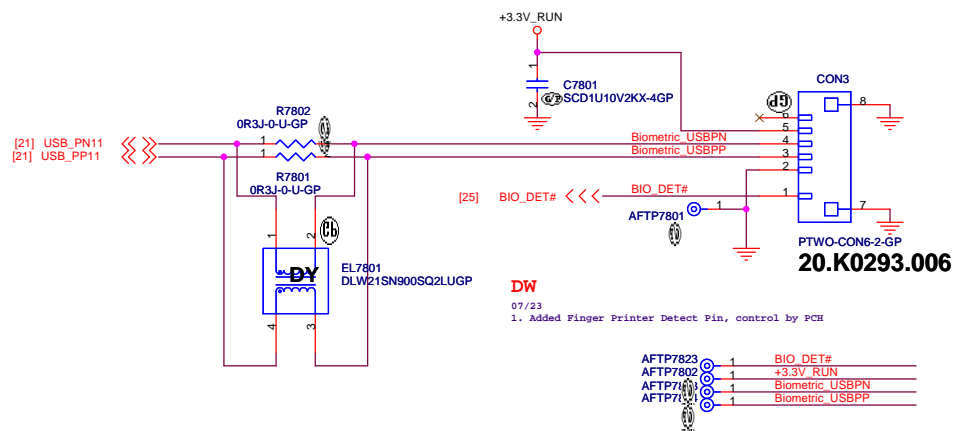
07/10 Change  
1. Change CON6 pin define, For Layout  
07/14 Updated Spec  
2. Deleted USB Port-5  
07/23  
1. Removed +1.5V\_RUN Power rail for JMB380  
2. Added CardReader Wake# to sent Card detect signal for PCH . ( Only For JMB380 )  
3. Change CON6 pin define  
07/28  
1. Added +5V\_ALW Power rail for Change Power & Battery LED  
from common-cathode to common-anode  
07/29  
1. Remove SATA2\_ACT\_LED  
08/05  
1. Changed CON6 Pin define  
08/11  
1. Changed CON6 Pin define  
2. Added +5V\_ALW for IO board  
08/18  
1. Added 48M clock for USB CardReader  
2. Added PCIE\_WAKE# signals for New Card  
3. Changed CON6 Pin define

+1.5V\_RUN : 650mA  
+3.3V\_RUN : 1775mA  
+3.3V\_ALW : 275mA  
+5V\_ALW : 60mA

<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Audio BD/IO BD CONN					
Size	Document Number				Rev
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## Finger Printer Connector



Added CON5 pin define	2009/05/26
Change CON5 pin define	2009/06/08
Change CON5 Pin define	2009/06/11
Revised CON5 Pin define	2009/06/17

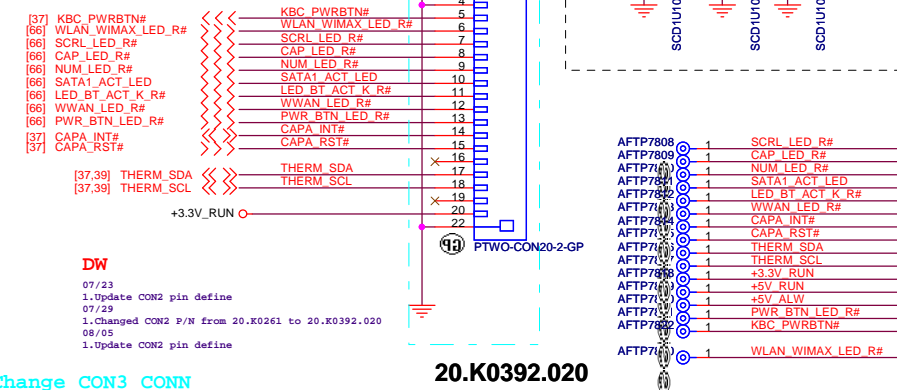
DW

07/10 Added  
1.Added Felica Connector

08/11 Removed  
1.Remored Felica Connector

## LED&amp;Capacity board CONN

Change LED  
signal name  
2009/06/01



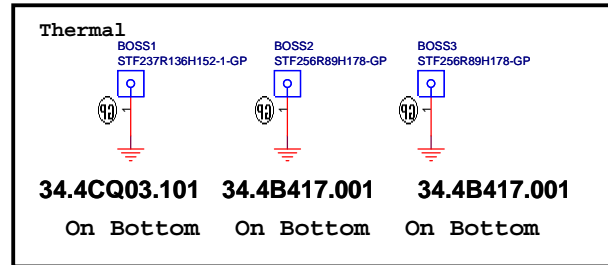
```
Change CON3 CONN
2009/06/01
Update CON pin define
2009/06/04
1. Moved 33ohm resistor, ESD diode to capacity BD
2. NC capacity BD RST pin
2009/06/09
Assign CAPA_RST# GPIO
2009/06/15
```

## <Core Design>

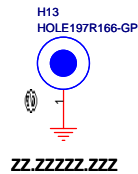


SSID = Mechanical

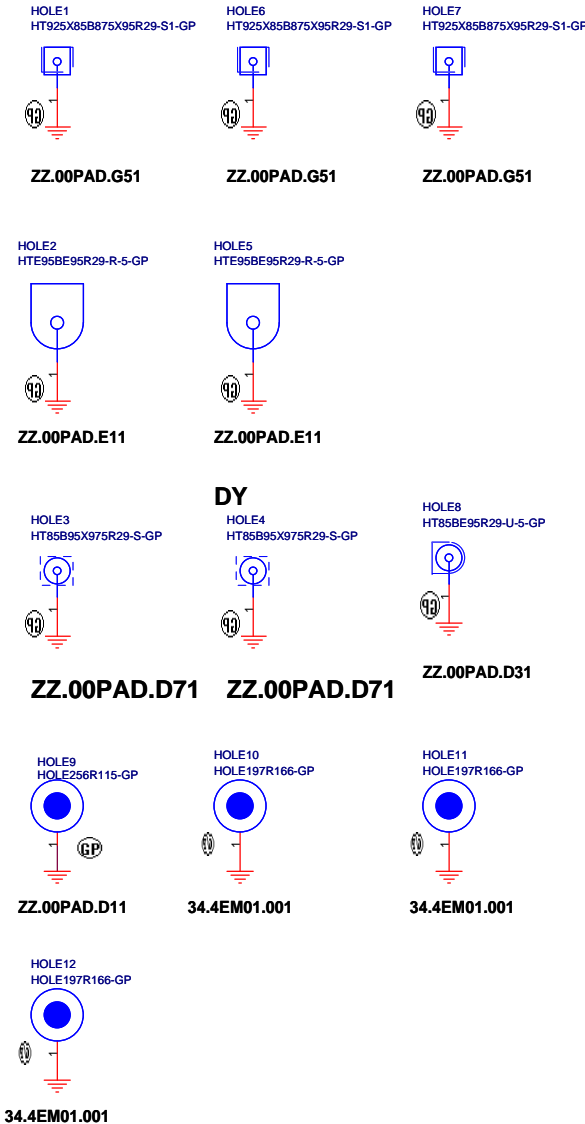
BOSS:



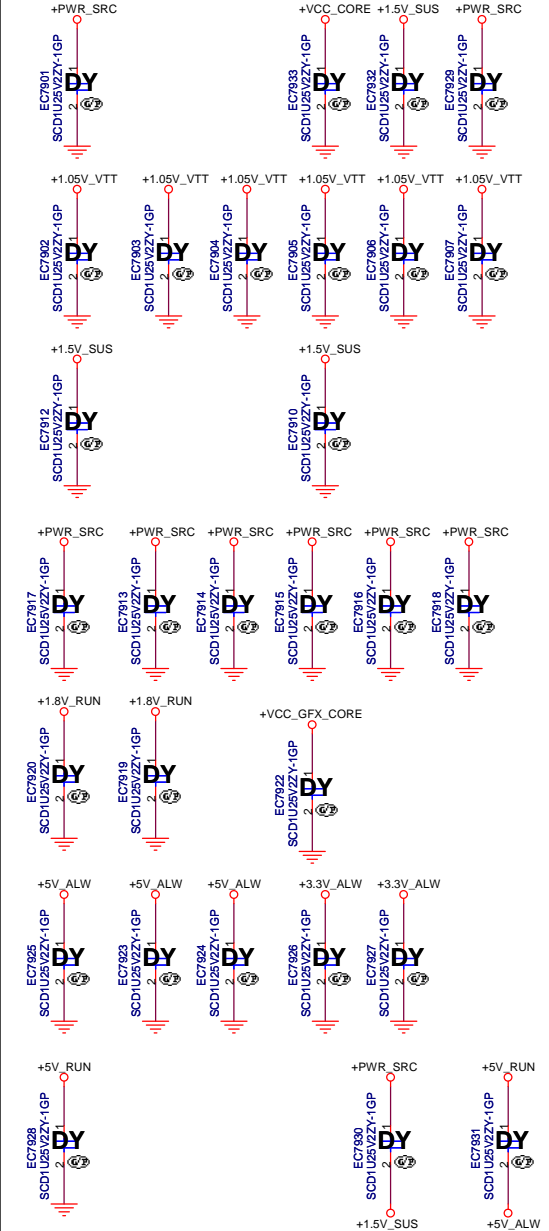
Boss modify 2009/07/23



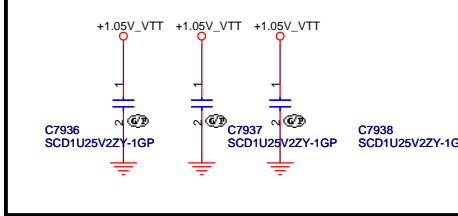
HOLE:



EMI Request



For DMI



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size Custom Document Number Rev

Vostro Calpella SA

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Title \_\_\_\_\_

VGA-PCI-E// VDS(1/4)

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**Vostro Calpella**

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		1		



**DW**

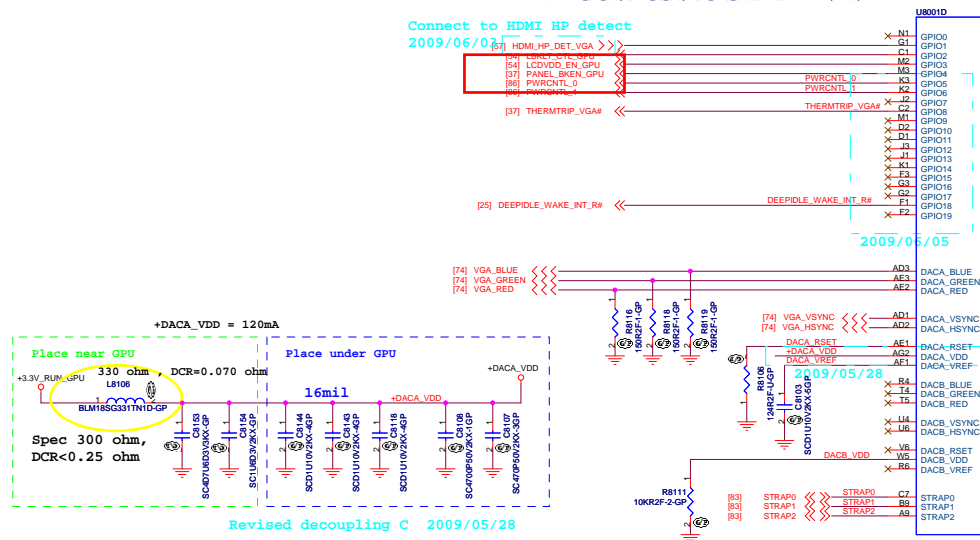
07/05

1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC

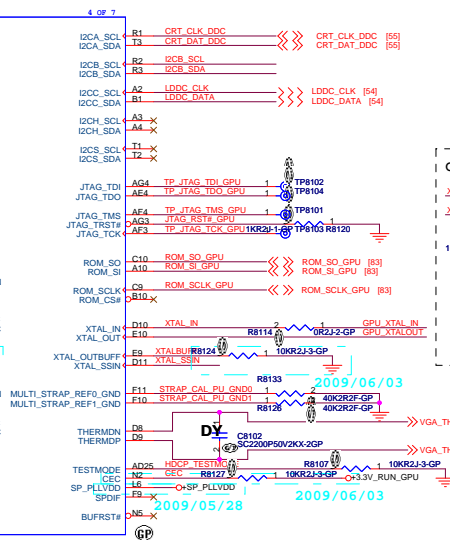
07/10 Not Reserve

1. Shorted LSKLT\_CTL1.GPU,LCDVDD\_EN.GPU,PANEL\_BKRN.GPU Not Reserve R8134,R8135,R8136

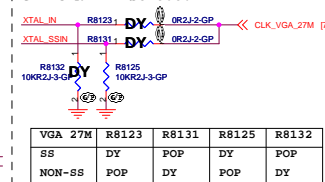
Connect to HDMI HP detect  
2009/06/03 [57] HDMI\_HP\_DET\_VGA >>>



Revised decoupling C 2009/05/28



```
| CLK GEN 27M select:
```



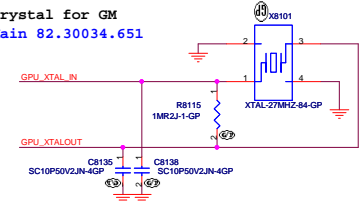
```

-----
Added CLK GEN 27M select circuit
Added R8132 (DY) 2009/06/17

```

Default X'TAL

```
| Crystal for GM
| Main 82.30034.
```



Place near GPU

+SP\_PLLVDD

+0.5V\_GFX\_PC

L8110

100nH+7-6P

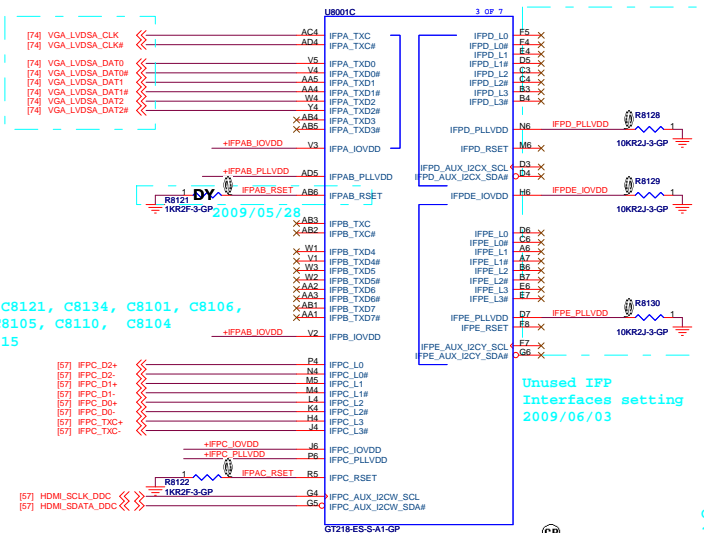
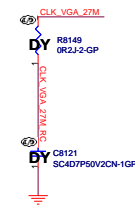
I SP\_PLLVDD=45mA

SC100V3X0-6P

SC470V03X00-6P

Revised decoupling C

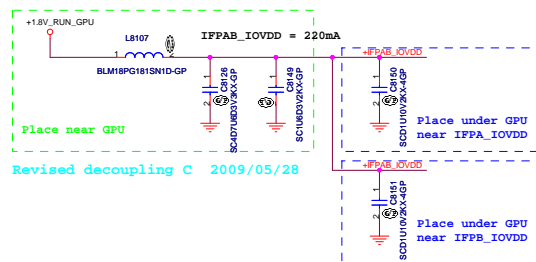
Revised decoupling C 2009/05/28



Removed C8121, C8134, C8101, C8106,  
C8114, C8105, C8110, C8104  
2009/06/15

Unused IFP  
Interfaces setting  
2009/06/03

```
+IFPAB_IOVDD
```

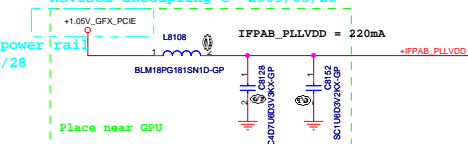


Revised decoupling C 2009/05/28

+IFPAB\_PLLVDD

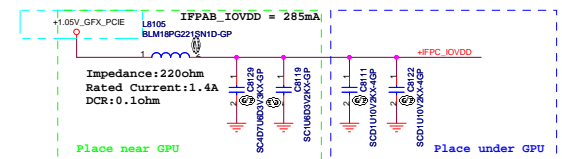
Revised decoupling C 2009/05/28

Change power  
2009/05/28



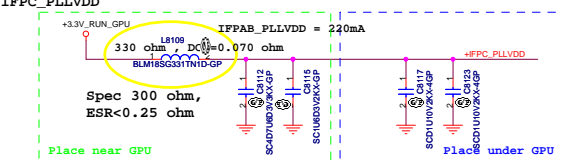
Place near GF

+IFPC\_IOVDD



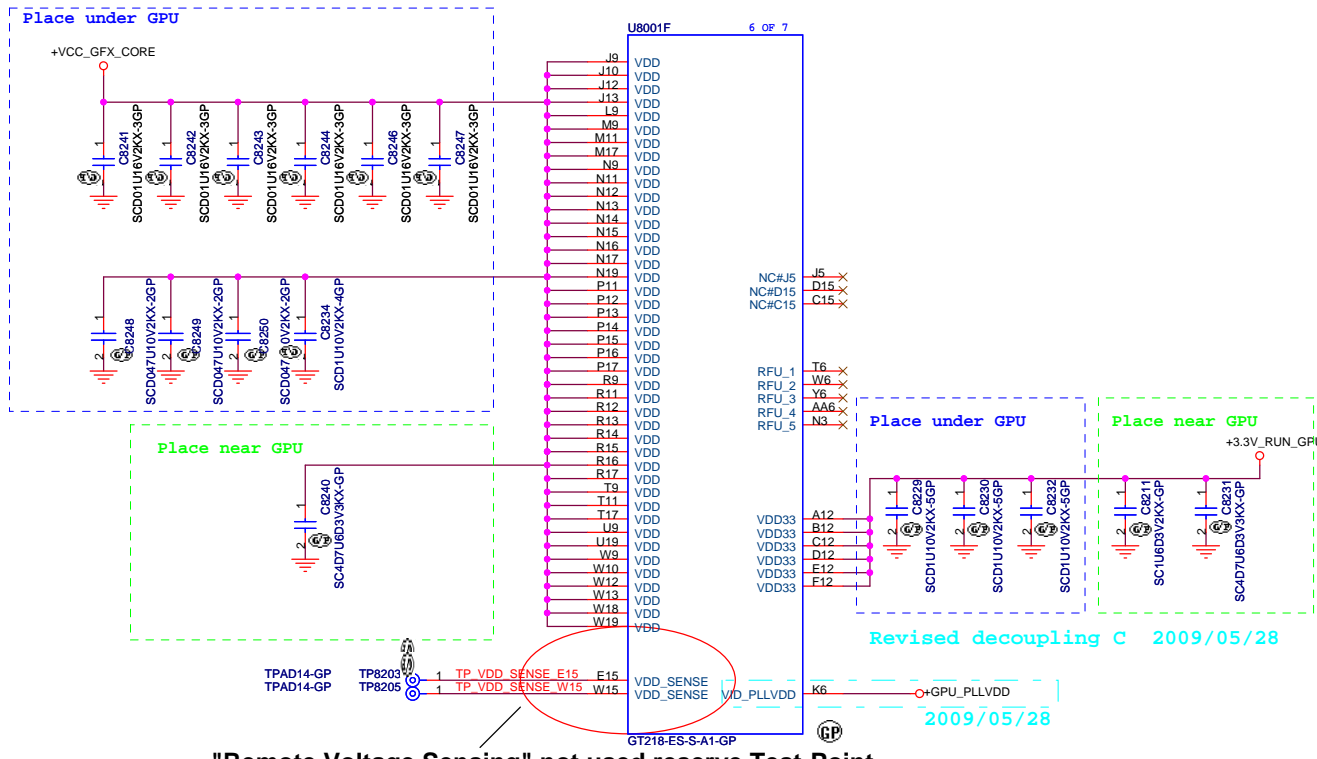
Revised decoupling G: 2009/05/23

+TFC PLI-VDD



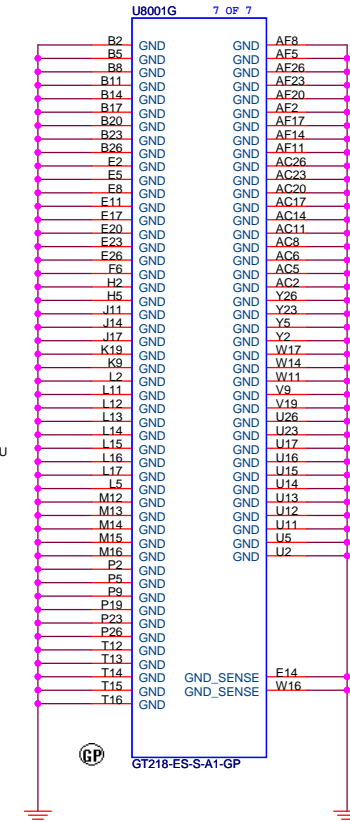
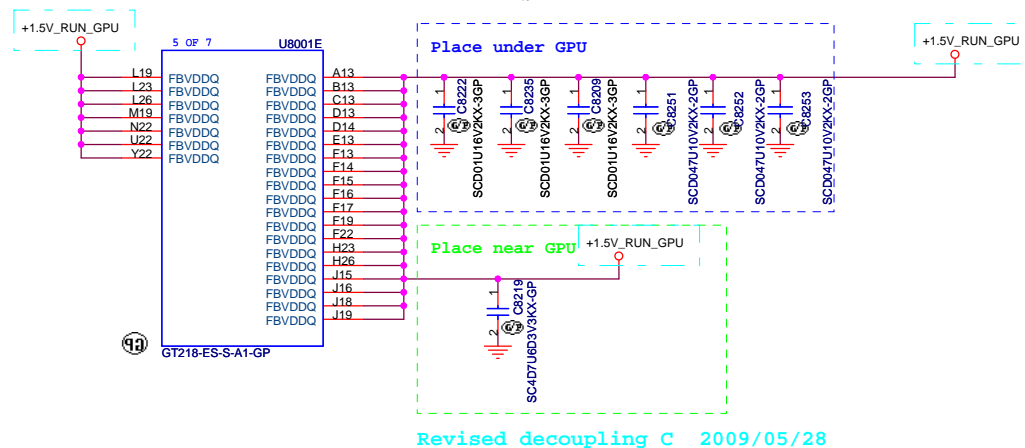
Received: September 4, 2000/05/00

Revised decoupling C 2009/05/28



"Remote Voltage Sensing" not used, reserve Test-Point.

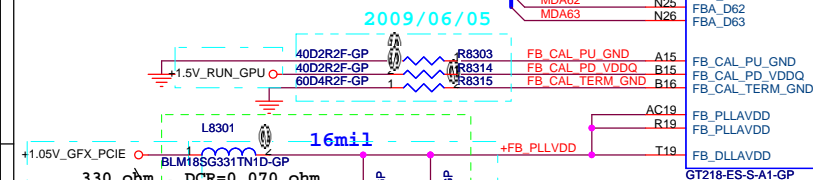
Change FBVDDQ power rail  
2009/05/28



<Core Design>

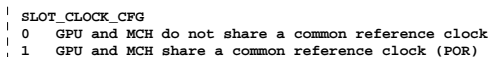
**DELL** Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			VGA-POWER/GND(3/4)		
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A3	Vostro Calpella				
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FB PLLAVDD+FB DLLAVDD=100mA

07/10 Updated  
1.+FB\_PLLVDD power rail corrected to +1.05V\_GFX\_PCIE



DELL

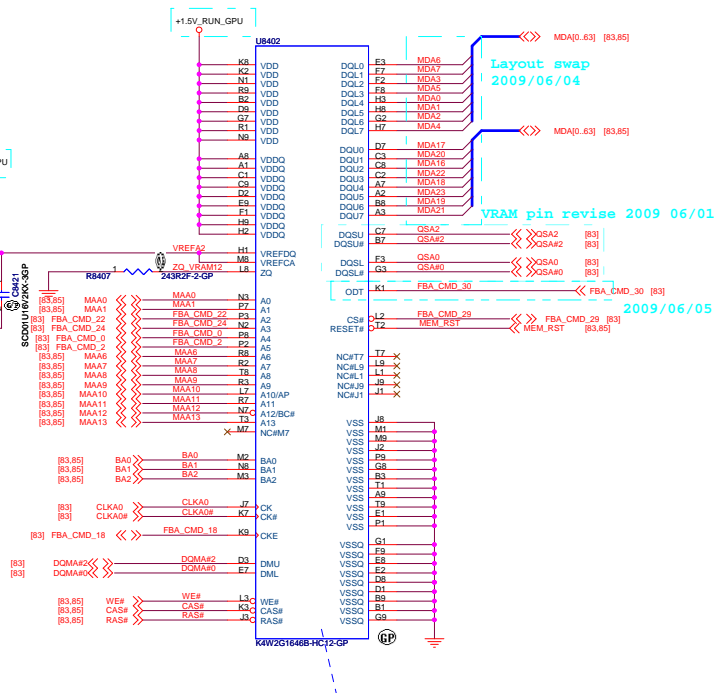
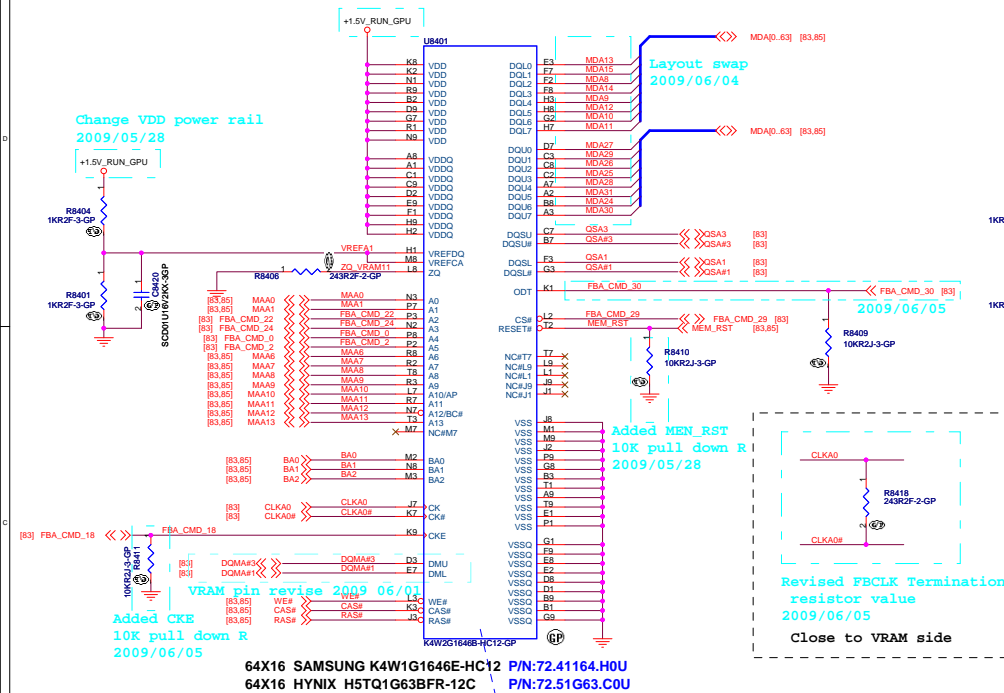
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

### VGA-MEMORY/STRAPS(4/4)

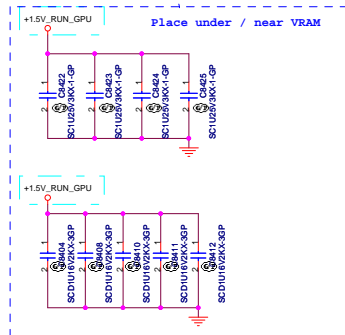
# Vostro Calpella

September 09, 2009 Sheet

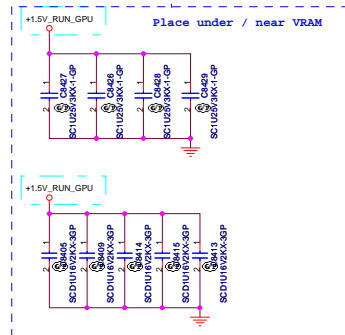
Rev



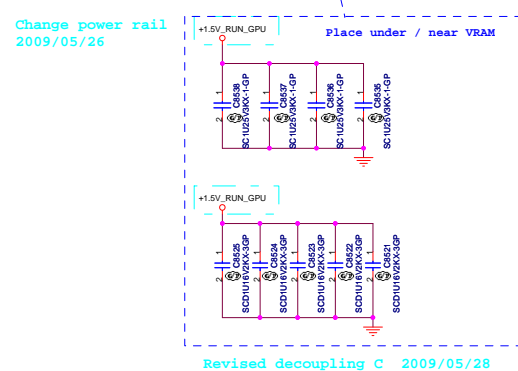
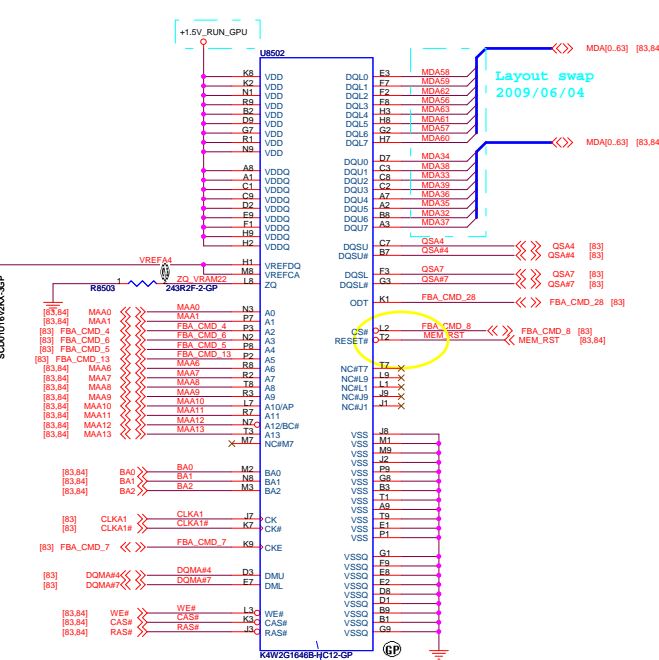
Change power rail  
2009/05/26



Change power rail  
2009/05/26



«Core Design»



$$V_{out} = 0.704V * (R1 + R2) / R2$$

DIS  
Thermal Design Current = 12.9A  
Max Current = 16.77A  
18.45A < OCP < 21.81A

Frequency setting  
470K --> 290KHz  
200K --> 340KHz  
100K --> 380KHz  
39K --> 430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V
L	L	0.8V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J  
O/P cap: 330U 2V EEP5X0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01  
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm@4.5Vgs/ 84.07686.037  
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mohm@4.5Vgs/ 84.00460.037  
Switching freq-->350KHz

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218 +VCC GFX CORE**

Size: Custom Document Number: **DW Calpella (Discrete)** Rev: **X00**

Date: Wednesday, September 09, 2009 Sheet: 66 of 88

### +3.3V\_RUN\_GPU:

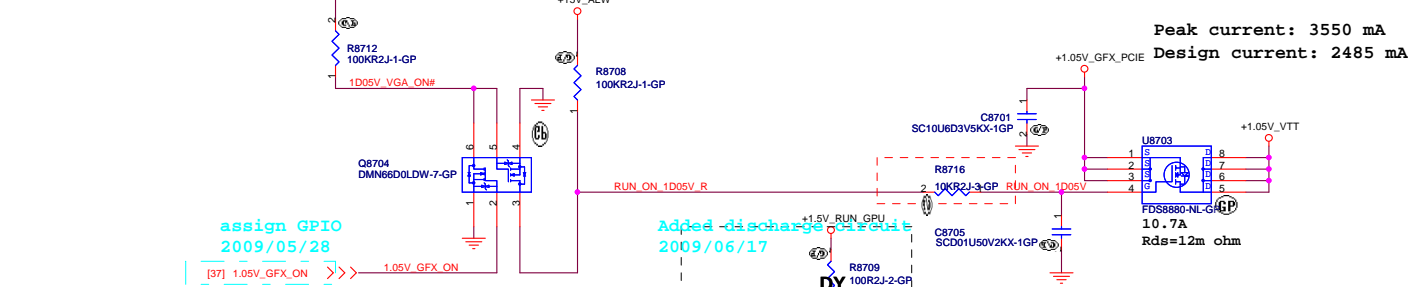
DW  
07/30  
1. Changed D8706 from 3-Pin to 2-Pin Diode, For saved more layout space



Peak current: 1140 mA  
Design current: 798 mA

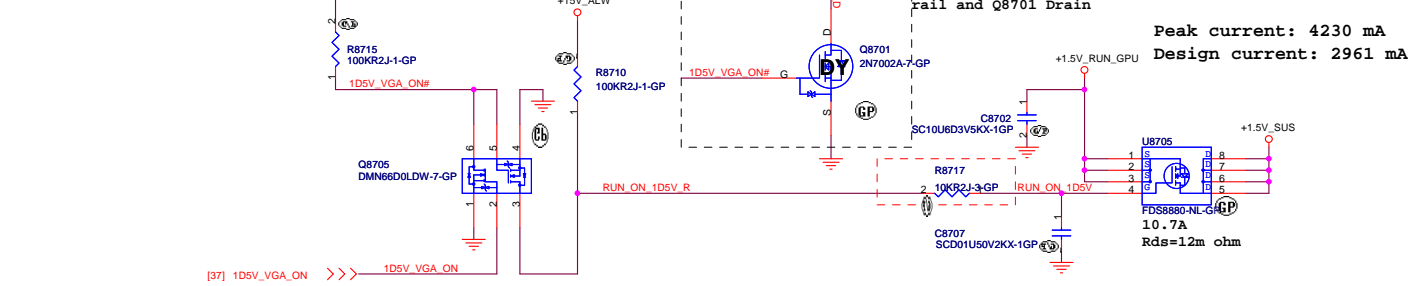
### +1.05V\_GFX\_PCIE:

assign GPIO  
2009/05/28



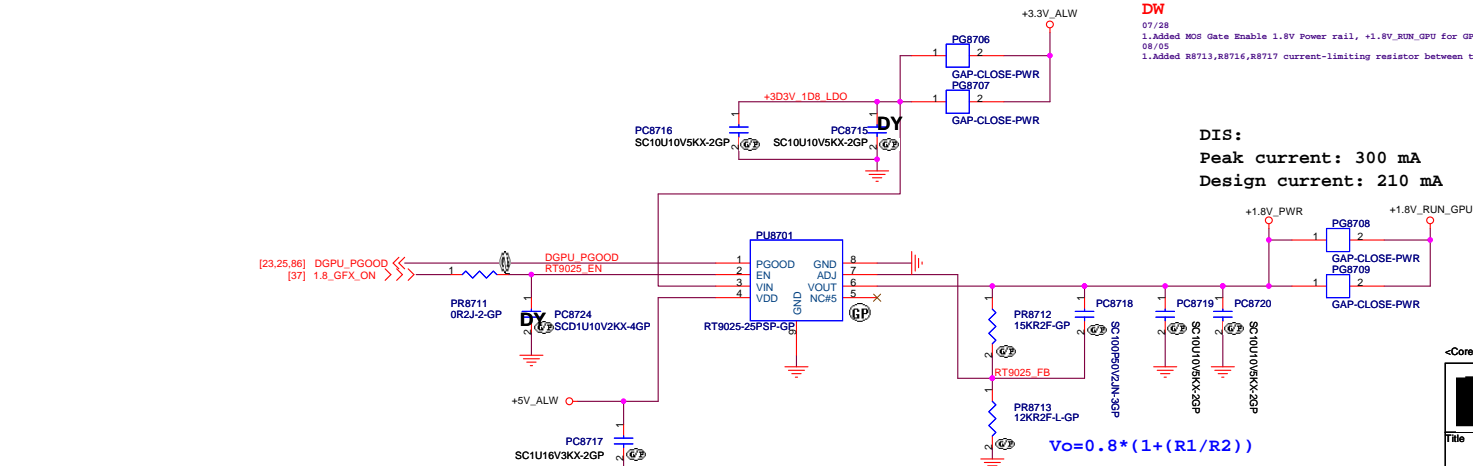
Peak current: 3550 mA  
Design current: 2485 mA

### +1.5V\_RUN\_GPU:



Peak current: 4230 mA  
Design current: 2961 mA

### +1.8V\_RUN\_GPU:



DW  
07/28  
1. Added MOS Gate Enable 1.8V Power rail, +1.8V\_RUN\_GPU for GPU  
08/05  
1. Added R8713, R8716, R8717 current-limiting resistor between the N-FET gate and turn on 12-V logic .

DIS:  
Peak current: 300 mA  
Design current: 210 mA

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>LDO 1.8V</b>	
Size	Document Number	Rev	
Custom	<b>Vostro Calpella</b>	SA	
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[illegible]